

ICs' hidden features enhance counter-based designs

ICs designed expressly for counter applications appear in most digital-device data books but might not offer the features you need. Chips dedicated to other applications, however, often include counter functions that you can access.

John Hatchett and William Morgan,
Motorola Semiconductor Products Sector

When looking for a digital counter, don't limit your search to dedicated ICs, which might require the "wrong" supply voltage, take too much power, operate too slowly or perhaps not be readily available. The function you need might be hidden within other devices aimed at different applications.

For example, frequency-synthesizer/phase-locked-loop ICs generally contain on-chip counters—often more than one. And CMOS-based versions of these devices tolerate wide supply-voltage variations, operate at low current levels and function at input frequencies in the tens-of-megahertz range.

Three devices provide the options

Three devices that meet these requirements, the MC145146, -151 and -157, each contain at least one 10-, 12- or 14-bit counter (Table 1) and operate over a 3 to 9V supply range. The counters' programming methods differ, suiting them to a variety of applications.

Table 2 shows the devices' counting ranges and counter-programming requirements: The 14-bit MC145151 accepts parallel counter loading; a 4-bit data bus programs the 10- and 12-bit -146 counters; and the -157's dual 14-bit counter loads via a clocked, serial data stream.

You parallel-load Fig 1a's MC145151 via inputs N_0 through N_{13} using Table 2's code sequence. (Note that all three devices achieve full count value for an all-ZERO input and are nonresponsive for inputs of 00...01 and 00...10.) By comparison, the -146's 10- and 12-bit counters require three 4-bit inputs at D_0 through D_3 (Fig 1b). Address bits A_0 through A_2 direct these 4-bit nibbles to the appropriate counter locations. The indicated strobe/chip-select signal (ST) allows the data and address lines to share a common bus with other

system functions because they achieve an inactive high-impedance state when ST is LOW.

The MC145157's dual 14-bit counters employ only three programming interface controls: the Data, Clock and Enable functions (Fig 1c). You accomplish a count-loading operation by clocking the data into the on-chip shift registers, then transferring the information into the latches by taking Enable HIGH. (Conversely, keeping Enable LOW allows you to enter new data into the registers without disturbing what's already in the counters.) The first 14 bits are the count value; the 15th bit selects which counter gets loaded—a ONE loads $\div R$, a ZERO loads $\div N$.

Other than these programming differences, the counters are sufficiently similar to permit one functional description, and an example application demonstrates their advantages.

A CMOS counter's current consumption generally depends on its supply voltage and the input's frequency

TABLE 1—COUNTER CHARACTERISTICS

OPERATING VOLTAGE	3 TO 9V DC
OPERATING TEMPERATURE	- 40 TO + 85°C
COUNTERS AVAILABLE:	
MC145146	ONE 12-BIT, ONE 10-BIT
MC145151	ONE 14-BIT
MC145157	TWO 14-BIT
TYPICAL CURRENT DRAIN AT 25°C FOR $I_{IN} = 10$ MHz, $V_{DD} = 5V$	
$V_{IN} = 2V$ p-p	2.0 mA DC
$V_{IN} = 0.5V$ p-p	2.4 mA DC
MAXIMUM F_{IN} WITH 500 mV P-P SINE-WAVE INPUT AND $V_{DD} = 5V$	15 MHz MIN
PACKAGE SIZE (DUAL IN-LINE):	
MC145146	20 PIN, 0.3-IN. WIDE
MC145151	28 PIN, 0.6-IN. WIDE
MC145157	16 PIN, 0.3-IN. WIDE

Programmable counters hide in chip block diagrams

and amplitude. Figs 2 and 3 show this relationship for the -151's 14-bit counter operating at 3 and 5V supply levels; they depict the results of using an external signal source, grounding the OSC_{IN} pin and leaving all other unused pins open. (Although you'll note slight

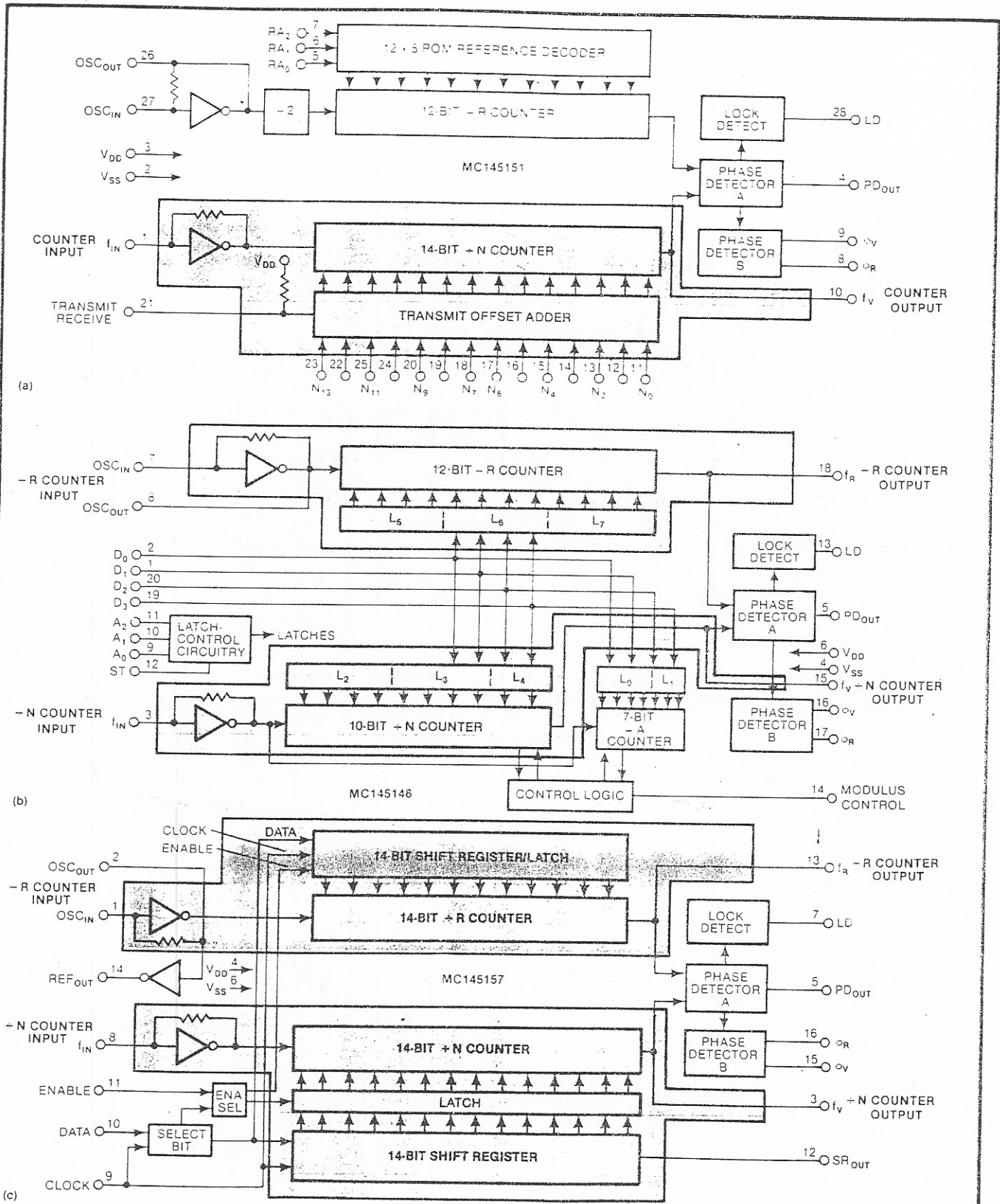


Fig 1—Programmable counters often hide within more complex ICs such as frequency-synthesizer/phase-locked-loop devices. For example, the MC145151 (a) includes a parallel-programmed 14-bit counter. The MC145146 chip (b) employs two counters—12- and 10-bit—driven by a 4-bit data bus, and the -157 (c) has dual counters programmed by 14-bit shift registers.

current
change
You
in co
coupl
input
at hig

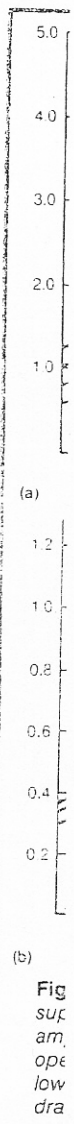


Fig 500 pro

hip for
supply
ternal
ing all
slight

current differences for different divider ratios, these changes are insignificant above approximately +32.)

You can supply a low-level (500 mV p-p) input signal in conjunction with the chip's built-in buffers and ac coupling; however, as Figs 2 and 3 indicate, a large input amplitude requires less supply current, especially at higher supply voltages. If your application operates

at standard CMOS logic levels, use direct coupling; if you employ ac coupling, be sure the waveform is symmetrical to avoid upsetting the on-chip bias levels, thus degrading the counter's sensitivity.

Fig 4 shows a counter's typical frequency capability over a -40 to +85°C span as a function of supply voltage and input-signal amplitude. Guaranteed maxi-

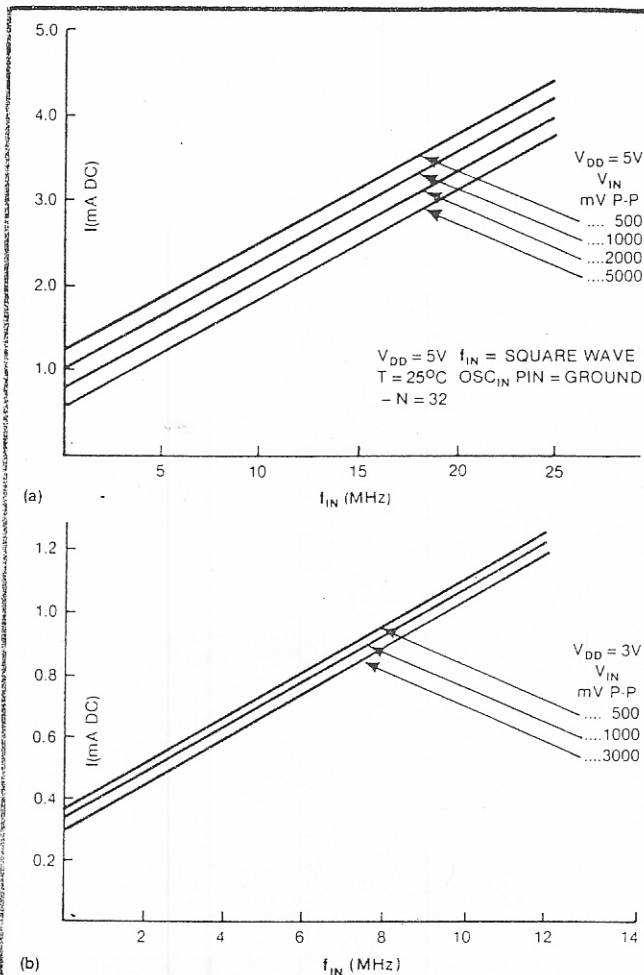


Fig 2—A CMOS counter's dc current drain depends on the supply voltage and the input signal's frequency and amplitude. Although a higher voltage does permit higher operating frequencies (a), it also causes higher currents at lower frequencies. For example, a 500-mV, 10-MHz input draws 2.4 mA at 5V (a) but only 1.1 mA at 3V (b).

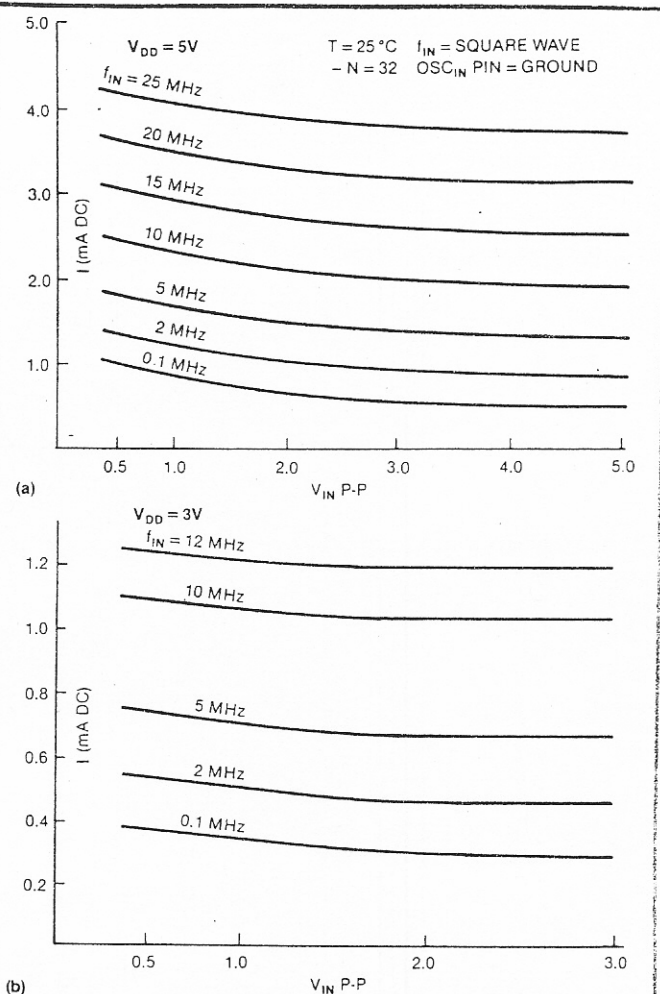


Fig 3—Varying a CMOS counter's input frequency has more of an effect on its supply current than does an input-amplitude change at a constant frequency. At divider values less than 32, the device's current requirements vary with its count requirements.

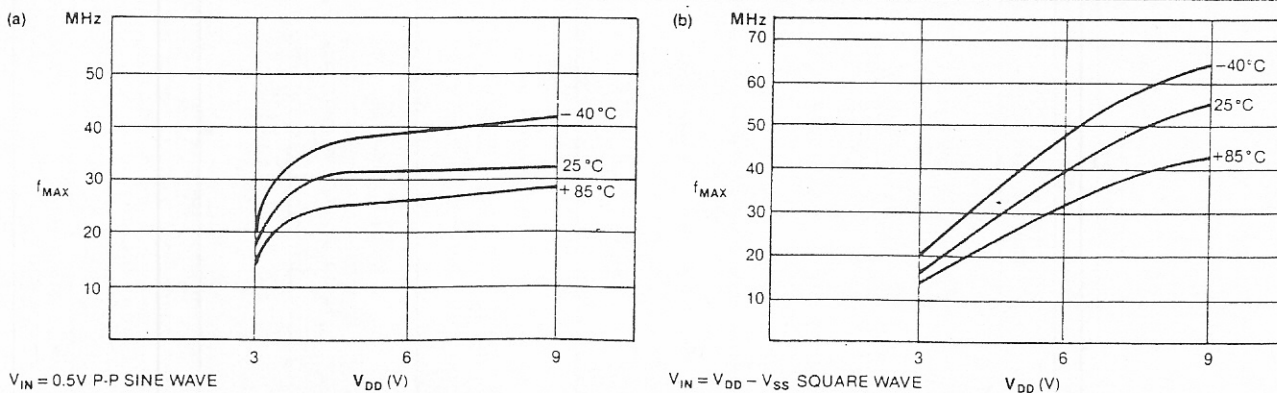


Fig 4—A counter's maximum operating frequency depends on its supply voltage, temperature and input signal amplitude. A 500-mV p-p sine-wave input (a) limits performance at the higher supply-voltage levels. A rail-to-rail square wave (b), however, provides impressive response at all supply levels.

