**Legacy Device:** *Motorola MC12034A*

The ML12034 can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola’s MC145xxx series or Lansdale’s ML145xxx series in a PLL to provide tuning signals up to 2.0 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- ML12034 for Positive Edge Triggered Synthesizers
- 12mA Maximum, -40 to 85°C, VCC = 5.5 Vdc
- Modulus Control Input is Compatible with Standard CMOS and TTL
- Low-Supply Current 8.5 mA Typical
- Operating Temperature Range £T_A£ = -40 to 85°C

**FUNCTIONAL TABLE**

<table>
<thead>
<tr>
<th>SW</th>
<th>MC</th>
<th>Divide Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>H</td>
<td>32</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>33</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>64</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>65</td>
</tr>
</tbody>
</table>

**NOTES:**
1. SW: H = VCC, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to VCC, L = Gnd to 0.8 V.

**MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Range</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage, Pin 2</td>
<td>VCC</td>
<td>-0.5 to 7.0</td>
<td>Vdc</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>£T_A£</td>
<td>-40 to 85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>£T_stg£</td>
<td>-65 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>Modulus Control Input, Pin 6</td>
<td>MC</td>
<td>-0.5 to 6.5</td>
<td>Vdc</td>
</tr>
</tbody>
</table>

**NOTES:**
1. ESD data available upon request.
2. This device contains protective circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, V_in and V_out should be constrained to the range Gnd ≤ (V_in or V_out) ≤ VCC.

**PIN CONNECTIONS**

In [Top View]

- In
- VCC
- SW
- OUT
- Gnd

Note: Lansdale lead free (Pb) product, as it becomes available, will be identified by a part number prefix change from ML to MLE.
### ELECTRICAL CHARACTERISTICS

$V_{CC} = 4.5$ to $5.5$ Vdc, $T_A = -40$ to $85^\circ$C, unless otherwise noted.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Toggle Frequency (Sin Wave)</td>
<td>$f_t$</td>
<td>0.5</td>
<td>2.4</td>
<td>2.0</td>
<td>GHz</td>
</tr>
<tr>
<td>Supply Current Output Unloaded (Pin 2)</td>
<td>$I_{CC}$</td>
<td>–</td>
<td>8.5</td>
<td>12</td>
<td>mA</td>
</tr>
<tr>
<td>Modulus Control Input High (MC)</td>
<td>$V_{IH1}$</td>
<td>2.0</td>
<td>–</td>
<td>$V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>Modulus Control Input Low (MC)</td>
<td>$V_{IL1}$</td>
<td>–</td>
<td>–</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Divide Ratio Control Input High (SW)</td>
<td>$V_{IH2}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>Vdc</td>
</tr>
<tr>
<td>Divide Ratio Control Input Low (SW)</td>
<td>$V_{IL2}$</td>
<td>Open</td>
<td>Open</td>
<td>Open</td>
<td>–</td>
</tr>
<tr>
<td>Output Voltage Swing ($C_L = 12$ pF, $R_L = 1.1$ kΩ)</td>
<td>$V_{out}$</td>
<td>1.0</td>
<td>1.6</td>
<td>–</td>
<td>$V_{pp}$</td>
</tr>
<tr>
<td>Modulus Setup Time MC to Out</td>
<td>$t_{SET}$</td>
<td>–</td>
<td>8.0</td>
<td>10.0</td>
<td>ns</td>
</tr>
<tr>
<td>Input Voltage Sensitivity 500 to 2000 MHz</td>
<td>$V_{in}$</td>
<td>100</td>
<td>–</td>
<td>1500</td>
<td>mVpp</td>
</tr>
<tr>
<td>Output Current ($C_L = 12$ pF, $R_L = 1.1$ kΩ)</td>
<td>$I_{O}$</td>
<td>–</td>
<td>–</td>
<td>3.5</td>
<td>mA</td>
</tr>
</tbody>
</table>

#### Figure 1. Logic Diagram

#### Figure 2. Modulus Setup Time

Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

#### Figure 3. Typical Output Waveform

- 500 mV
- 20 ns
Figure 4. AC Test Circuit

Sine Wave Generator

C1

50 Ω

C2

VCC

SW

C3

In

Out

MC

MC Input

Gnd

External Components
C1 = C2 = 1000 pF
C3 = 0.1 μF
CL = 12 pF (Including Scope and JIG Capacitance)
RL = 1.1 kΩ

VCC = 4.5 Vdc to 5.5 Vdc

Figure 5. Input Signal Amplitude versus Input Frequency

Figure 6. Output Amplitude versus Input Frequency
Figure 7. Generic block diagram showing prescaler connection to PLL device

Figure 7 shows a generic block diagram of connecting a prescaler to a PLL device that supports dual modulus control. Application note AN535 describes using a two-modulus prescaler technique. By using a prescaler higher frequencies can be achieved than by a single CMOS PLL device.
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