Adding to PLL chips' functions speeds rf synthesizer design

Programmable phase-locked-loop ICs contain reference oscillator and divide-down counters, offer dual-modulus prescaling

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☐ A new family of large-scale integrated circuits is now available to provide those designing rf synthesizers with breakthroughs in performance, power drain, cost, and space. Each chip in the family provides large blocks of phase-locked-loop circuitry, thus reducing the effort in designing all kinds of radio-frequency equipment. By using complementary-MOS technology, this family of circuits has the added appeal of drawing a minimum of power over a wide range of supply voltages.

Applications abound for these easily implemented phase-locked-loop ICs. They include avionics, navigation and communications equipment, mobile radio transceivers, marine radio and sonobuoys, amateur radios, scanner receivers, cable and broadcast television tuning systems, and a-m/fm radios.

Each member of the MC145100 family of PLL synthesizer chips contains a reference oscillator, a selectable reference-frequency divider, a digital phase detector with a lock-detection output, and at least one programmable divide-by-N counter.

Some of the chips have a dual-modulus prescaling capability for extended frequency range (see "Dual-modulus prescaling"). With the loop filter, voltage-controlled oscillator, and suitable dual-modulus prescaler needed to complete the PLL circuit, these ICs can synthesize frequencies to over 500 megahertz.

Frequency is selected by programming the divide-by-N and, where applicable, the divide-by-A counters with either a serial bit stream, a fully parallel word (14 or 16 bits wide), or coding on a 4-bit bus. The family's variety of frequency-selection schemes and other on-chip features allow the designer to minimize the need for additional components for an application (see Table 1).

Highlights of the synthesizer family are:

- 30-MHz input capability (typical at 25°C, 5 volts dc).
- Operation at 3 to 9 volts dc.
- Low power drain.
- −40° to +85°C operating temperature.
- Linear detector response.
- Low input drive level (500 millivolts peak to peak).
- On-chip latches and shift registers for serial and 4-bit-bus designs.

Interfacing the frequency synthesizers with microprocessor or microcomputer controllers is best accomplished employing the chips offering serial or 4-bit-wide inputs; the parallel-programmed devices interface best with mechanical switches, diode matrixes, and programmable read-only memories. The parallel input designs are housed in 0.6-inch-wide, 28-pin packages, and the other units come in narrow-lead-frame, 0.3-in.-wide, 16-, 18-, or 20-pin packages.

There are seven chips in the family. Each of the three programming methods (serial, parallel, and 4-bit data bus) is represented by both a single- and a dual-modulus

TABLE 1: FEATURES OF THE MC145100 FREQUENCY-SYNTHESIZER CHIP FAMILY

Programming method	Features	Part number	Modulus	Number of pins
4-bit data bus	• latches • enable/chip-select • software-programmed reference divider	MC145144	single	16
		MC145145	single	18
		MC145146	dual	20
Fully parallel	• pull-up resistors on all programming lines	MC145151 (receive/transmit shift function)	single	28
		MC145152	dual	28
Serial bit stream	• shift registers • latches • enable • latched outputs for use as system switching functions	MC145155	single	18
		MC145156	dual	20

Dual-modulus prescaling

Dual-modulus prescaling, used with three of the MC145100 family of large-scale integrated circuits, is a well-established method for designing high-performance high-frequency synthesizers. The technique allows the relatively low-frequency programmable counters on the synthesizer chip (the divide-by-A and divide-by-N functions of the MC145156, -52 and -46 devices) to function as a single high-frequency programmable counter. Actually, the lower-frequency counters on these ICs are used to control external high-speed chips called dual-modulus prescalers. The prescaler consists of one or sometimes two ICs made for this purpose. This control is done with the aid of special logic on the LSI chip for selecting one of two prescaler division values, either P or P + 1.

The division control signal generated by the synthesizer chip is supplied to the prescaler in a specific, timed format: the division value is P + 1 while A is counting down and P when A has stopped and N is counting the rest of the way down. Thus the low-frequency on-chip counters control the high-frequency prescaler. Note that $N \geq A$ is a requirement for using dual-modulus prescaling.

The greater the total system division value, N_{total}, the higher the output frequency of the synthesizer. N_{total} is a function of three input values: the prescaler division value, P; the value of A, programmed into the divide-by-A counter; and the value of N, programmed into the divide-by-N counter. The relationship is:

$$N_{total} = NP + A$$

To see how this equation is applied, consider the problem of tuning a radio receiver. A maximum resolution over the widest possible frequency range is desirable. For the minimum frequency increment, N is therefore held constant and A is varied between 0 and P − 1 in integral steps. N is then incremented to N + 1 and A is again incremented sequentially from 0 to P − 1. In effect, the system performs tuning in two stages—first coarse, then fine. The procedure is used over the entire N_{total} range. The actual tuning increment is equal to the reference frequency, f_R. Without dual-modulus prescaling—that is, with fixed prescaling—the tuning increment is $P' \times f_r$, where P′ is the division value for the fixed prescaler.

A dual-modulus prescaler can operate up to the speed capability of the prescaler chip without sacrificing system resolution or performance, which would occur if a fixed (single-modulus) divider was used for the prescaler. High frequency is achievable because the dual-modulus prescaler must divide by only two different values (P or P + 1) and can therefore be designed for high operating speeds comparable to those of fixed dividers.

Motorola's dual-modulus prescaler chips, off-the-shelf parts, offer speeds to over 500 megahertz. They are used individually or in some cases combined with an additional counter IC to provide a variety of P and P + 1 values to best serve the application at hand. Figures 4 and 5 (pp. 153 and 154, respectively) show two examples.

The 145156, -52, and -46 chips can control prescaler division values that range from 3 and 4 through 128 and 129 (for the -56 and -46 devices) or 3 and 4 through 64 and 65 (for the -52).

version, and chips with 4-bit-wide data input include an extra single-modulus version designed specifically for television tuner applications, bringing the total number of chips to seven. Figure 1 depicts the internal functions of the chips, the variations available, and the external components required to complete the PLL. Table 2 summarizes the chips' basic characteristics.

Dual-modulus requirements

The MC145156, -52, and -46 are for use in synthesizers that employ the dual-modulus prescaling concept. Each contains the circuitry for all the lower-frequency functions, along with the modulus control signal for operating the prescaler in the divide-by-P or divide-by-P + 1 mode in the properly timed format for performance to over 500 MHz.

Synthesizing high frequencies using the dual-modulus concept requires a special high-speed counter, or prescaler. By matching a synthesizer chip with one or more of the ICs that make up the prescaler (Motorola makes a series of them), a designer may tailor a system to meet a variety of speed, performance, and cost goals.

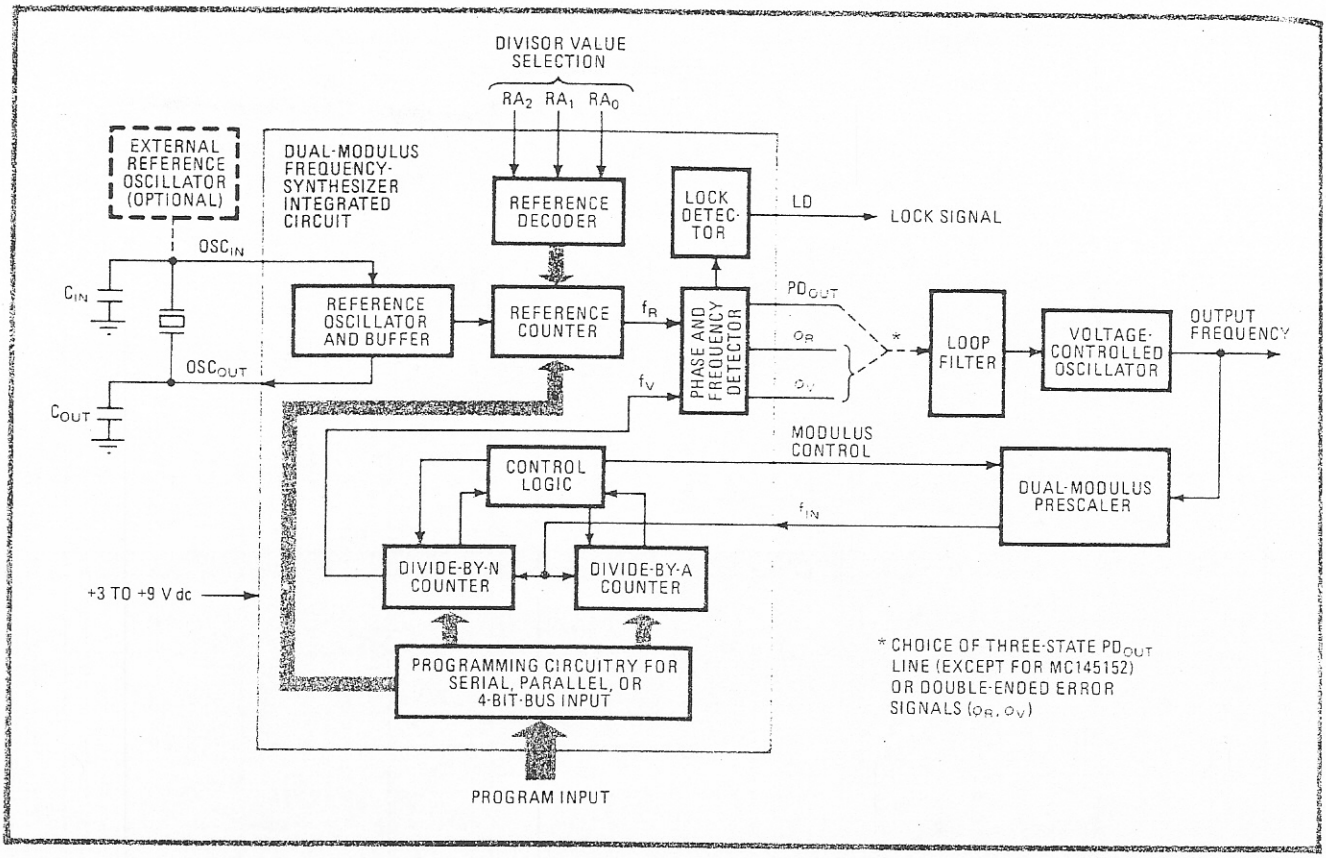
The MC145156 and -46 contain 10-bit divide-by-N and 7-bit divide-by-A counters and can control prescalers having division values (P and P + 1) ranging from 3 and 4 through 128 and 129. Depending on the prescaler selection, a range from 9 to 131,199 in steps of unity can be achieved for the total system division value, N_{total}. The availability of only 6 bits in the MC145152's divide-by-A counter restricts it to controlling prescalers having division values of 3 and 4 through 64 and 65. In this case, the upper N_{total} limit is limited to 65,599.

The other four devices, the MC145155, -51, -45, and -44 are used when programmability at higher frequencies using dual-modulus prescaling is not required. Since a modulus control signal is not generated, these ICs employ a single counter for the divide-by-N function. Except for the MC145144, the counter contains 14 bits and can be programmed to divide by 3 through 16,384. The 145144, although similar to the -45, is optimized specifically for TV tuning system designs and employs a fixed divide-by-256 prescaler.

Typical frequency characteristics are given in Fig. 2. As shown in Fig. 2a, the use of high-amplitude drive levels will have little effect on the maximum operating frequency for drain supply voltages, V_{DD}, less than about 5 V. However, for higher V_{DD} levels, high drive levels can increase the maximum frequency significantly.

Current drain is predominantly set by the counters and the driving-signal frequencies. Except at extremely low frequencies, the other on-chip functions will produce only secondary current-drain effects. This results in about the same total drain current value, I_{DD}, for all members of the family under the same operating conditions. From Figs. 2b and 2c a characteristic plot of I_{DD} as a function of voltage and frequency can be drawn to determine the current requirements with large-amplitude (rail-to-rail) input signals.

With low-amplitude drive levels (500 mV p-p), the current will remain essentially as shown in Figs. 2b and



1. Integrated. The MC145100 family of C-MOS frequency synthesizer chips contain the bulk of the circuitry needed to implement a phase-locked-loop design. Dual-modulus prescaling for higher-frequency operation is optional on three of the family's seven members.

2c for a V_{DD} of 3 V. For the 5- and 9-V conditions and for operating frequencies in excess of a few hundred kilohertz, higher current drain results.

The reference oscillator and buffer on each chip is used for developing a crystal-controlled reference signal by connecting an external fundamental-mode crystal that is parallel-resonant at the desired operating frequency and by loading the crystal with two capacitors, C_{in} and C_{out}, to ground (see Fig. 1 again).

The acceptable loading capacitance, C_L, seen by the crystal depends upon the oscillator frequency. For a V_{DD} of 5 V, C_L should not exceed 32 picofarads for frequencies up to approximately 8 MHz, 20 pF for frequencies in the range of 8 to 15 MHz, and 10 pF for frequencies above 15 MHz.

These guidelines for C_L take into account IC-capacitance drive capability, variations in stray and IC input/output capacitance, and realistic crystal load-capacitance values. The load capacitance, C_L, presented across the crystal can be estimated to be a $C_{in\ total}$ in series with a $C_{out\ total}$, where:

$$C_{in\ total} = C_{in} + C_{in\ IC} + C_{in\ stray}$$

$$C_{out\ total} = C_{out} + C_{out\ IC} + C_{out\ stray}$$

with $C_{in\ IC}$ and $C_{in\ stray}$ representing the capacitance to ground at OSC_{in} contributed by the integrated circuit and stray circuit effects, respectively. Similarly, $C_{out\ IC}$ and $C_{out\ stray}$ apply to the OSC_{out} pin. C_{in} and C_{out} are capacitors that are added to achieve the proper C_L value. They should be chosen to make $C_{in\ total}$ and $C_{out\ total}$ approximately equal. In practice, C_{in} and C_{out} will be nominally equal. The oscillator can be trimmed to frequency by making a portion or all of C_{in} variable.

The 145156, -55, and -45 provide a buffered oscillator output, REF_{out}, for use in other system functions. For the 145152, -51, and -46, the oscillator signal can also be obtained by lightly coupling to OSC_{out}. This can be done by using a capacitor-tap impedance-transformation network for C_{out}.

An off-chip reference source can also be used to drive the oscillator input. The reference signal is applied to OSC_{in} and the crystal, and C_{in} and C_{out} are omitted. The oscillator circuitry now behaves as a buffer amplifier. The external reference signal will typically be ac-coupled to OSC_{in}, but for high-amplitude signals (standard C-MOS logic levels), dc coupling may be used.

The reference counter's role

The reference counter divides down the high-frequency reference signal to the desired comparison frequency, f_R, which is fed into the phase detector. When using the 145156, -55, -52, and -51, the user chooses one of eight possible division values with a 3-bit code applied to division-value select pins RA_0, RA_1, and RA_2,

The reference counters in the 145146 and -45 are fully user-programmable for integers 3 through 4,096 with a 12-bit binary code. Typically, the desired division value is selected by software through a microprocessor or microcomputer interface with the synthesizer's 4-bit-bus programming structure.

The digital phase-frequency detector on the synthesiz-

er chips compares positive-going edges of its two phase-compared input signals (f_R and f_V) and generates output error signals PD_{out}, ϕ_R, and ϕ_V as pulses of varying widths whenever the f_R and f_V edges are not in alignment (Fig. 3).

The error signals are filtered by the loop filter and thus establish the control voltage for a voltage-controlled oscillator. Except with the 145152 and -44, the user is provided a choice of either double-ended (ϕ_R, ϕ_V) or single-ended (PD_{out}) error information. The -52 offers only ϕ_R and ϕ_V and the -44 only PD_{out}.

Outputs ϕ_R and ϕ_V are well suited for use with loop filters that provide common-mode rejection and summing properties such as those employing operational amplifiers. PD_{out} is a three-state output and presents a high impedance and a minimum of error-signal energy to be filtered when the loop is locked—in other words, when f_R and f_V are equal in frequency and phase.

Previous detectors for frequency-synthesizer applications have typically exhibited large changes in gain (sometimes changing by an order of magnitude) near the zero, or phase-lock, point. This can result in many system design difficulties and compromises in loop performance. The detector used in the 145100 chips produces a linearized response that provides a relatively constant detector gain through the phase-lock region and synthesizer performance better than that of previous designs.

The user can maintain some flexibility in indicating an in-lock or out-of-lock condition by using the lock-detection output. When the loop is locked, a lock-detection pin, LD, is high except for a narrow low-level pulse (normally 100 nanoseconds wide for a V_{DD} of 5 V). When the loop is not locked, LD pulses low during the time an error signal of either polarity is generated (see Fig. 3 again). Typically, output LD is integrated and used to bias a transistor switch on and off. In this way, the user can assign the point when a phase-lock condition is actually to be indicated.

Programmable counters, too

The 145155, -51 and -45 contain a single 14-bit counter for the divide-by-N function. Those that control an external dual-modulus prescaler—the 145156, -52, and -46—must have this function made up of two separate counters. This is implemented using a 10-bit counter, designated divide-by-N, and either a 7-bit or 6-bit (145152) counter, designated divide-by-A. In addition, a fully programmable 12-bit reference counter is provided in the 145145 and -46. The division value of each counter corresponds to the number (in binary code) applied to the counter's programming inputs. The only exceptions are when binary codes having a value of less than 3 are applied to the divide-by-N and reference counters. For these cases, a binary zero code gives a division value of 2^b, where b is the number of bits of the counter. Division values for binary codes of 1 and 2 are not specified.

All the counters are preceded by buffer stages to allow the use of low-amplitude inputs (500 mV p-p) when ac coupling is used. If a large-amplitude signal is available (standard C-MOS logic levels), dc coupling may also be used. For optimum performance when ac coupling is employed, input signals should be symmetrical.

TABLE 2: CHARACTERISTICS OF THE MC145100 FAMILY OF FREQUENCY-SYNTHESIZER CHIPS

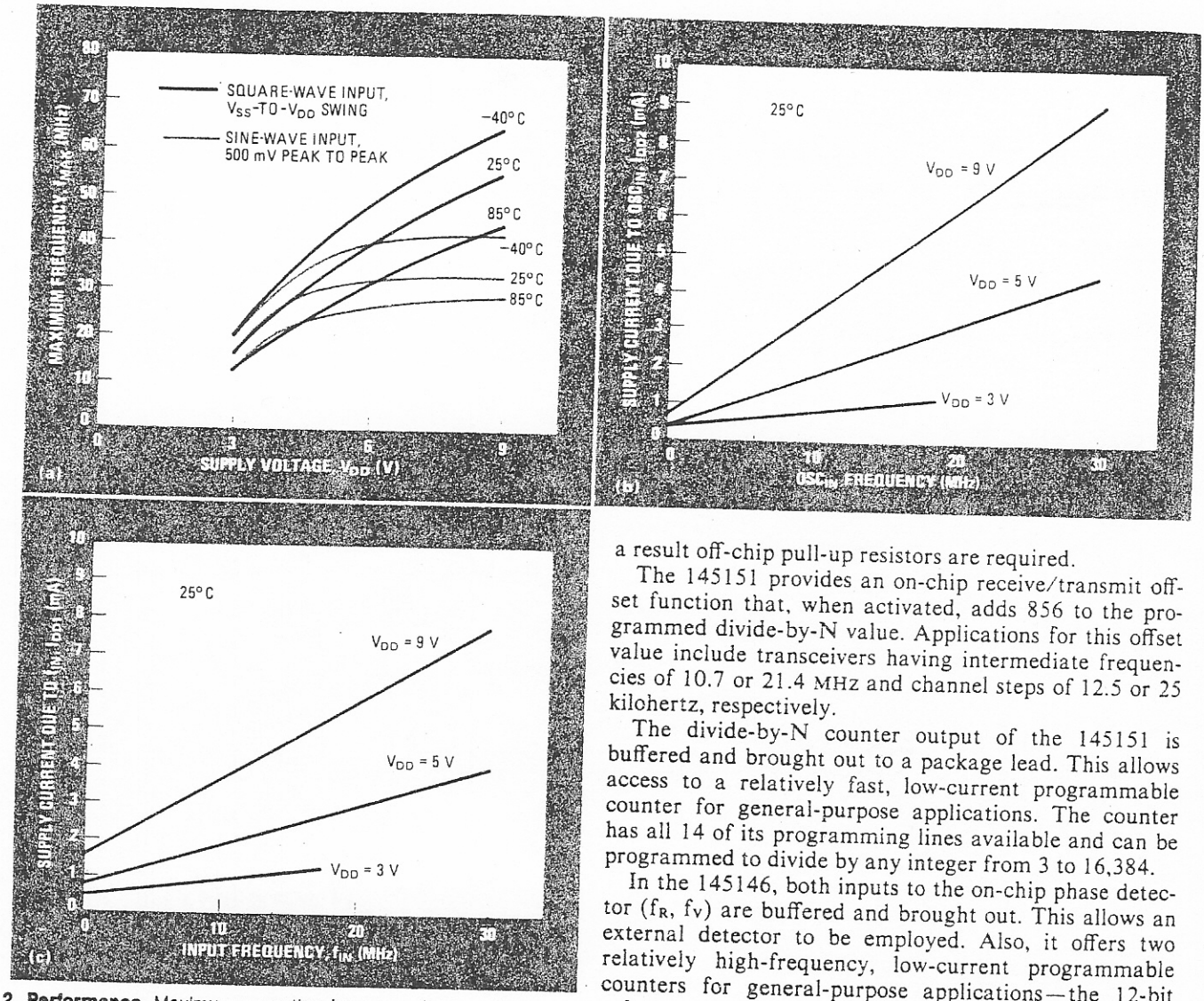
Operating voltage	3 to 9 V dc
Typical current drain, with f_{IN} = OSC_{IN} = 10 MHz and V_{DD} = 5 V, at 25°C	4 mA dc
Operating temperature	−40° to +85°C
Maximum f_{IN}, with 500-mV peak-to-peak sine wave and V_{DD} = 5 V	15 MHz minimum
System frequency	> 500 MHz
Dual-modulus prescaler range	
MC145156, -46	divide by 3 or 4 through 128 or 129
MC145152	divide by 3 or 4 through 64 or 65
Maximum total division value (N_{TOTAL}) with dual-modulus prescaling	
MC145156, -46	131,199
MC145152	65,599
Time required to generate modulus control signal, at 25°C, with V_{DD} = 5 V	50 ns typical, 100 ns maximum
Divide-by-N range, MC145145, -51, and -55	3 through 16,384

The control logic generates the modulus control signal. This signal is used to establish the divide-by-P and divide-by-P + 1 format of an external dual-modulus prescaler and therefore allows the 145156, -52, and -46 to function in dual-modulus prescaling modes.

The modulus control is dc-coupled to the prescaler's control input and will interface directly with most existing dual-modulus prescaling ICs. The prescaler should divide by P for a high signal on its control line and by P + 1 for a low signal. The prescaler's output should make a low-to-high transition after each group of P or P + 1 input cycles to the prescaler. This action provides the proper interface to the positive-edge–triggered divide-by-A and divide-by-N counters, maximizing the time available for generating the modulus control signal and thus optimizing system frequency capability.

The modulus control signal is low at the beginning of a count cycle and remains low until the divide-by-A counter has counted down from its programmed value, A. At that time, the modulus control signal is set high and remains high until the divide-by-N counter has counted the rest of the way down from its programmed value, N. This will be N − A additional counts, since both divide-by-N and divide-by-A counters are decrementing during the beginning of the cycle. The modulus control signal is then set back low, the counters are preset to their respective programmed values, and the sequence is repeated. This order of timed events results in a total programmable divide value for the system defined by $N_{total} = N \times P + A$, where $N \geq A$.

When using dual-modulus prescaling, the maximum input frequency, f_{in}, for the 145156, -52, or -46 is usually not limited by the speed capability of the divide-by-A or divide-by-N counter, but is dictated by the propagation time through the prescaler (period a), the prescaler's control-input setup or release time (period b), and the



2. Performance. Maximum operating frequency (a) is achieved by increasing both supply and drive-signal voltages. Current drain is primarily a function of reference oscillator frequency (b) and input frequency (c). The total current is the sum of I_{DD1} and I_{DD2}.

time required for the LSI synthesizer to generate the modulus control signal (period c).

The f_{in} signal must be low enough in frequency so that its period is greater than the sum of periods a, b, and c. Two of these factors (a and b) are determined by the user's dual-modulus prescaler implementation. Period c is a factor determined by the LSI device and is typically 50 ns for a V_{DD} of 5 V (see Table 2 again).

For added flexibility, both the 145155 and -56 provide two latched open-drain outputs, SW_1 and SW_2, for system switching functions. These functions are controlled by the first 2 bits in the serial data stream used to program the ICs and may be used in any way to aid the designer or enhance the system.

A logic 1 in the control bit causes the respective switch output to assume a high-impedance state, and a logic 0 causes the output to sink current and provide a low impedance. Both switches use an open-drain configuration capable of controlling dc levels to over 15 V, and as a result off-chip pull-up resistors are required.

The 145151 provides an on-chip receive/transmit offset function that, when activated, adds 856 to the programmed divide-by-N value. Applications for this offset value include transceivers having intermediate frequencies of 10.7 or 21.4 MHz and channel steps of 12.5 or 25 kilohertz, respectively.

The divide-by-N counter output of the 145151 is buffered and brought out to a package lead. This allows access to a relatively fast, low-current programmable counter for general-purpose applications. The counter has all 14 of its programming lines available and can be programmed to divide by any integer from 3 to 16,384.

In the 145146, both inputs to the on-chip phase detector (f_R, f_V) are buffered and brought out. This allows an external detector to be employed. Also, it offers two relatively high-frequency, low-current programmable counters for general-purpose applications—the 12-bit reference counter and the 10-bit divide-by-N counter. Both are programmed using a 4-bit data-bus structure.

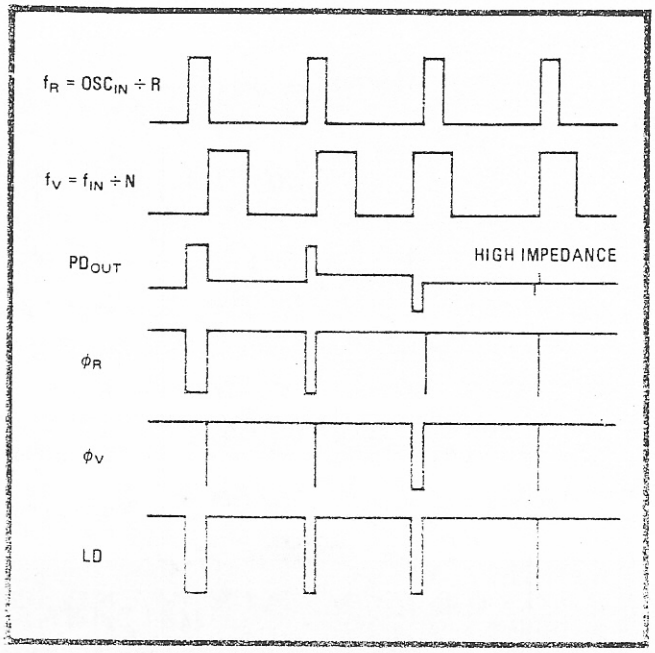
Programming the counters

The serial and 4-bit–bus devices are typically used in systems employing a microprocessor or microcomputer for the programming interface. The parallel units can serve in these applications also but are frequently at a disadvantage because they require a large number of interface connections.

For the serial devices, the 145155 and -56, programming involves only three interface lines: the data, clock, and enable lines. Programming is accomplished by clocking data serially into the on-chip shift registers and then transferring their contents into latches with the enable line. Each low-to-high clock transition causes the registers to shift right 1 bit as each data bit is shifted in on the data pin at the time of the clock transition. (As mentioned, the first 2 bits control the two open-drain switch outputs, SW_1, and SW_2, instead of programming the counters.)

An inhibiting feature, activated by holding enable low, allows new data to be entered without affecting the previously programmed information. The programming

3. Phase-locked. When the divided-down frequencies of the reference oscillator and the input are locked in phase, the detector output assumes a high-impedance state; the double-ended outputs and the lock-detector ouput are reduced to narrow slivers.



interface can be reduced to only two lines, the data and clock lines, by holding the enable line high. However, under this condition all program changes are continuously transferred to the latches and counters, resulting in erroneous information being entered during the programming time-frame. Depending on the application, such errors may or may not be acceptable.

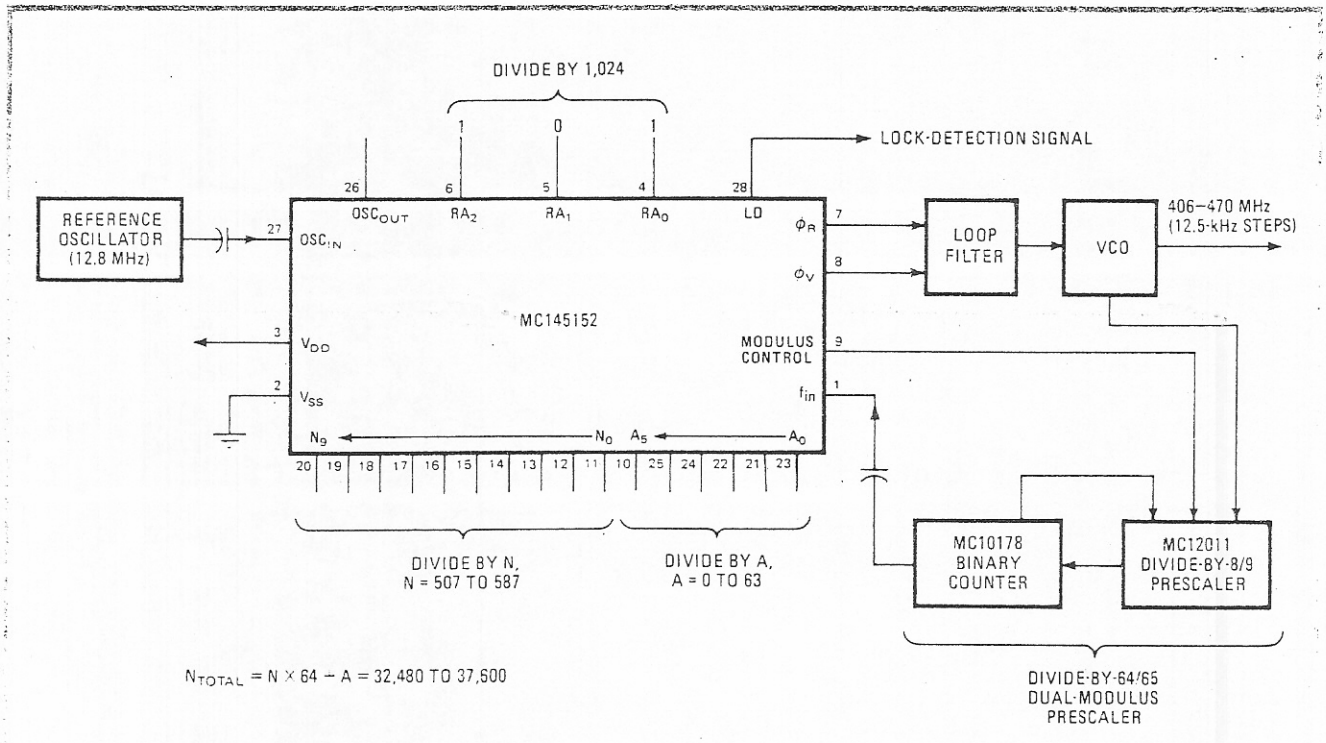
A fully parallel input

For parallel devices 145151 and -52, all counter programming points are brought out to the package pins. Programming is accomplished by taking the appropriate pins high or low. There are 14 programming lines for the MC145151 (14-bit divide-by-N counter) and 16 for the -52 (10-bit divide-by-N and 6-bit divide-by-A counters). In applications in which lines will not be changed, they can be hardwired to the appropriate level. Built in pull-up resistors are provided on all the programming inputs.

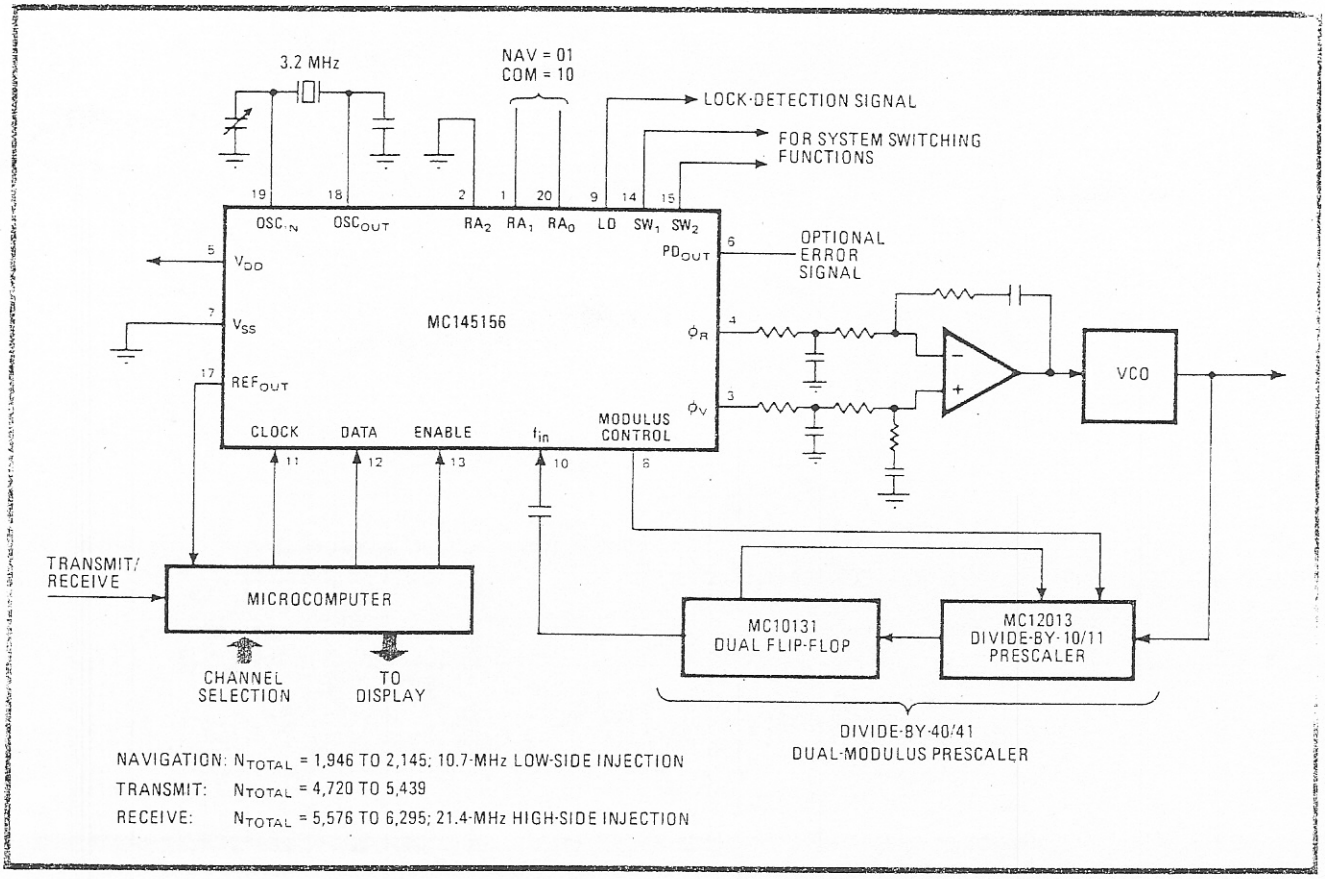
Finally, for the 145145 and -46, which use 4-bit data buses, programming is done using eight interface lines—four for the data word, three for the address that directs data to one of eight latches (seven for the -45), and one for an enable/chip-select function. Although eight lines are involved, only the chip-select line, ST, must be dedicated to the synthesizer chip. The remaining seven can share the bus with other system functions, since they assume an inactive, high-impedance state when ST is held low. They need to be activated only when programming changes are made.

Three data words program the reference divider. Five data words are used to program the divide-by-N and divide-by-A counters in the 145146, and four words program the divide-by-N counter in the -45. The addressable on-chip latches store the information between program changes.

The 145100 chips can be used in a variety of synthe-



4. Uhf. Good tuning ability is easily implemented at ultrahigh frequencies. With the reference-divider code inputs RA_0, RA_1, and RA_2 set as shown, the reference oscillator division value is 1,024. Frequency can be stepped in 12.5-kHz increments for the 12.8-MHz oscillator shown.



5. Multifunction. Both navigation and communication functions are incorporated in a single synthesizer. Different tuning increments are programmed into the reference frequency divider and a microcomputer serially programs the division values of the counters.

sizer designs. Figures 4 and 5 show samples of some possible implementations. Any of the three programming methods discussed can usually be chosen without major concept changes.

Applications

Figure 4 illustrates an approach for a high-frequency synthesizer employing dual-modulus prescaling intended for an ultrahigh-frequency mobile radio. As with all PLL frequency synthesizers, a comparison, or reference, frequency is compared in phase with the output of a voltage-controlled oscillator, and any difference generates a corrective signal that is fed to the VCO.

The countdown circuits discussed earlier allow the output frequency of the VCO to be many multiples of the comparison frequency. The exact multiple equals the effective division value of the countdown circuits between the phase detector and the VCO. Thus, changing the division value changes the output frequency, making the circuit tunable in discrete increments. Using the dual-modulus prescaling technique as shown in Fig. 4, the VCO tuning-increment resolution is equal to the comparison frequency, f_R, fed into the phase detector—in this example, 12.5 kHz.

Dual-modulus prescaling ICs with a maximum-frequency specification in excess of 500 MHz over the temperature range of −55° to +125°C are available. These devices may be used individually or combined with an additional divider to increase the prescaling divide factor and thus lower the input frequency, f_{in}, to a value within the specifications of the LSI device. The MC10178 and MC10131 emitter-coupled-logic ICs in Figs. 4 and 5 perform this function.

For the navigation or communication synthesizer in Fig. 5, it is also possible to use a TTL device for the dual–flip-flop function in the prescaler. To facilitate this, an on-chip ECL-to-TTL translator is available in some dual-modulus prescaler ICs such as the MC12009, -11, and -13. In the circuit shown, the VCO's output ranges from 97.300 to 107.250 MHz in 50-kHz steps; for communications transmission, it is 118.000 to 135.975 MHz in 25-kHz steps; and for reception, it is 139.400 to 157.375 MHz, also in 25-kHz steps.

The 145145 and −46 synthesizer chips provide the user with the access to fully program the 12-bit reference divider for values from 3 to 4,096. This feature can be used to obtain divide-by-R values not available with other family members. Selecting a divide-by-R value allows the frequency of the reference oscillator to be chosen to serve multiple functions, such as the injection signal for a receiver's second mixer stage.

Another feature of these two chips is that they require only one dedicated program line. This is because four data lines and three address lines can share the data-bus system with other ICs. This sharing makes multiloop synthesizer designs more practical. Three or even more loops may be controlled without undue complexity at the programming interface. □