

# Adding to PLL chips' functions speeds rf synthesizer design

Programmable phase-locked-loop ICs contain reference oscillator and divide-down counters, offer dual-modulus prescaling

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□ A new family of large-scale integrated circuits is now available to provide those designing rf synthesizers with breakthroughs in performance, power drain, cost, and space. Each chip in the family provides large blocks of phase-locked-loop circuitry, thus reducing the effort in designing all kinds of radio-frequency equipment. By using complementary-MOS technology, this family of circuits has the added appeal of drawing a minimum of power over a wide range of supply voltages.

Applications abound for these easily implemented phase-locked-loop ICs. They include avionics, navigation and communications equipment, mobile radio transceivers, marine radio and sonobuoys, amateur radios, scanner receivers, cable and broadcast television tuning systems, and a-m/fm radios.

Each member of the MC145100 family of PLL synthesizer chips contains a reference oscillator, a selectable reference-frequency divider, a digital phase detector with a lock-detection output, and at least one programmable divide-by-N counter.

Some of the chips have a dual-modulus prescaling capability for extended frequency range (see "Dual-modulus prescaling"). With the loop filter, voltage-controlled oscillator, and suitable dual-modulus prescaler needed to complete the PLL circuit, these ICs can synthesize frequencies to over 500 megahertz.

Frequency is selected by programming the divide-

by-N and, where applicable, the divide-by-A counters with either a serial bit stream, a fully parallel word (14 or 16 bits wide), or coding on a 4-bit bus. The family's variety of frequency-selection schemes and other on-chip features allow the designer to minimize the need for additional components for an application (see Table 1).

Highlights of the synthesizer family are:

- 30-MHz input capability (typical at 25°C, 5 volts dc).
- Operation at 3 to 9 volts dc.
- Low power drain.
- -40° to +85°C operating temperature.
- Linear detector response.
- Low input drive level (500 millivolts peak to peak).
- On-chip latches and shift registers for serial and 4-bit-bus designs.

Interfacing the frequency synthesizers with microprocessor or microcomputer controllers is best accomplished employing the chips offering serial or 4-bit-wide inputs: the parallel-programmed devices interface best with mechanical switches, diode matrixes, and programmable read-only memories. The parallel input designs are housed in 0.6-inch-wide, 28-pin packages, and the other units come in narrow-lead-frame, 0.3-in.-wide, 16-, 18-, or 20-pin packages.

There are seven chips in the family. Each of the three programming methods (serial, parallel, and 4-bit data bus) is represented by both a single- and a dual-modulus

TABLE 1 FEATURES OF THE MC145100 FREQUENCY SYNTHESIZER CHIP FAMILY

Programming method	Features	Part number	Modulus	Number of pins
4-bit data bus	<ul style="list-style-type: none"> <li>• latches</li> <li>• enable/chip-select</li> <li>• software-programmed reference divider</li> </ul>	MC145144	single	16
		MC145145	single	18
		MC145146	dual	20
Fully parallel	<ul style="list-style-type: none"> <li>• pull-up resistors on all programming lines</li> </ul>	MC145151 (receive/transmit shift function)	single	28
		MC145152	dual	28
Serial bit stream	<ul style="list-style-type: none"> <li>• shift registers</li> <li>• latches</li> <li>• enable</li> <li>• latched outputs for use as system switching functions</li> </ul>	MC145155	single	18
		MC145156	dual	20

## Dual-modulus prescaling

Dual-modulus prescaling, used with three of the MC145100 family of large-scale integrated circuits, is a well-established method for designing high-performance high-frequency synthesizers. The technique allows the relatively low-frequency programmable counters on the synthesizer chip (the divide-by-A and divide-by-N functions of the MC145156, -52 and -46 devices) to function as a single high-frequency programmable counter. Actually, the lower-frequency counters on these ICs are used to control external high-speed chips called dual-modulus prescalers. The prescaler consists of one or sometimes two ICs made for this purpose. This control is done with the aid of special logic on the LSI chip for selecting one of two prescaler division values, either  $P$  or  $P + 1$ .

The division control signal generated by the synthesizer chip is supplied to the prescaler in a specific, timed format: the division value is  $P + 1$  while  $A$  is counting down and  $P$  when  $A$  has stopped and  $N$  is counting the rest of the way down. Thus the low-frequency on-chip counters control the high-frequency prescaler. Note that  $N \geq A$  is a requirement for using dual-modulus prescaling.

The greater the total system division value,  $N_{total}$ , the higher the output frequency of the synthesizer.  $N_{total}$  is a function of three input values: the prescaler division value,  $P$ ; the value of  $A$ , programmed into the divide-by-A counter; and the value of  $N$ , programmed into the divide-by-N counter. The relationship is:

$$N_{total} = NP + A$$

To see how this equation is applied, consider the prob-

lem of tuning a radio receiver. A maximum resolution over the widest possible frequency range is desirable. For the minimum frequency increment,  $N$  is therefore held constant and  $A$  is varied between 0 and  $P - 1$  in integral steps.  $N$  is then incremented to  $N + 1$  and  $A$  is again incremented sequentially from 0 to  $P - 1$ . In effect, the system performs tuning in two stages—first coarse, then fine. The procedure is used over the entire  $N_{total}$  range. The actual tuning increment is equal to the reference frequency,  $f_r$ . Without dual-modulus prescaling—that is, with fixed prescaling—the tuning increment is  $P' \times f_r$ , where  $P'$  is the division value for the fixed prescaler.

A dual-modulus prescaler can operate up to the speed capability of the prescaler chip without sacrificing system resolution or performance, which would occur if a fixed (single-modulus) divider was used for the prescaler. High frequency is achievable because the dual-modulus prescaler must divide by only two different values ( $P$  or  $P + 1$ ) and can therefore be designed for high operating speeds comparable to those of fixed dividers.

Motorola's dual-modulus prescaler chips, off-the-shelf parts, offer speeds to over 500 megahertz. They are used individually or in some cases combined with an additional counter IC to provide a variety of  $P$  and  $P + 1$  values to best serve the application at hand. Figures 4 and 5 (pp. 153 and 154, respectively) show two examples.

The 145156, -52, and -46 chips can control prescaler division values that range from 3 and 4 through 128 and 129 (for the -56 and -46 devices) or 3 and 4 through 64 and 65 (for the -52).

version, and chips with 4-bit-wide data input include an extra single-modulus version designed specifically for television tuner applications, bringing the total number of chips to seven. Figure 1 depicts the internal functions of the chips, the variations available, and the external components required to complete the PLL. Table 2 summarizes the chips' basic characteristics.

### Dual-modulus requirements

The MC145156, -52, and -46 are for use in synthesizers that employ the dual-modulus prescaling concept. Each contains the circuitry for all the lower-frequency functions, along with the modulus control signal for operating the prescaler in the divide-by- $P$  or divide-by- $P + 1$  mode in the properly timed format for performance to over 500 MHz.

Synthesizing high frequencies using the dual-modulus concept requires a special high-speed counter, or prescaler. By matching a synthesizer chip with one or more of the ICs that make up the prescaler (Motorola makes a series of them), a designer may tailor a system to meet a variety of speed, performance, and cost goals.

The MC145156 and -46 contain 10-bit divide-by- $N$  and 7-bit divide-by- $A$  counters and can control prescalers having division values ( $P$  and  $P + 1$ ) ranging from 3 and 4 through 128 and 129. Depending on the prescaler selection, a range from 9 to 131,199 in steps of unity can be achieved for the total system division value,  $N_{total}$ . The availability of only 6 bits in the MC145152's divide-by- $A$  counter restricts it to controlling prescalers having

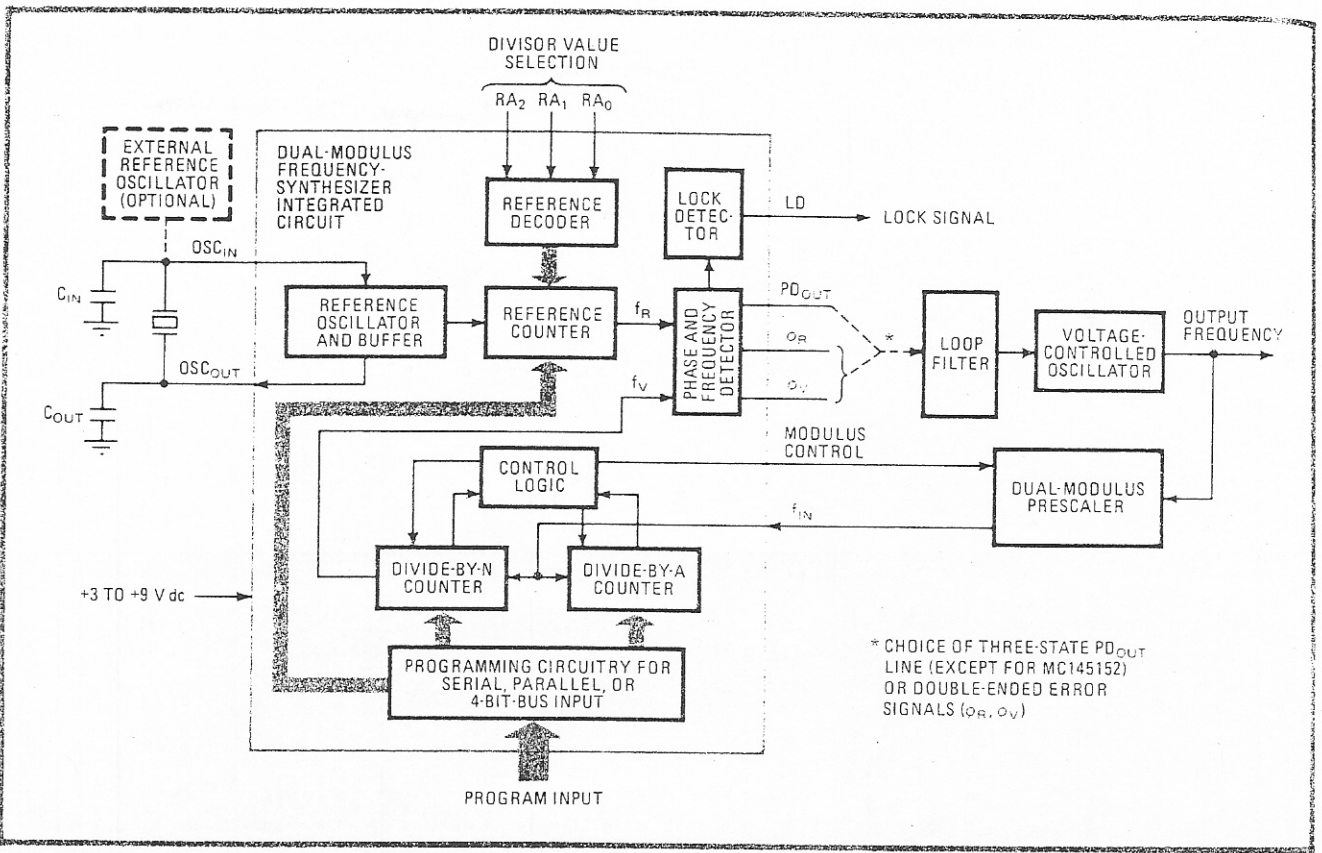
division values of 3 and 4 through 64 and 65. In this case, the upper  $N_{total}$  limit is limited to 65,599.

The other four devices, the MC145155, -51, -45, and -44 are used when programmability at higher frequencies using dual-modulus prescaling is not required. Since a modulus control signal is not generated, these ICs employ a single counter for the divide-by- $N$  function. Except for the MC145144, the counter contains 14 bits and can be programmed to divide by 3 through 16,384. The 145144, although similar to the -45, is optimized specifically for TV tuning system designs and employs a fixed divide-by-256 prescaler.

Typical frequency characteristics are given in Fig. 2. As shown in Fig. 2a, the use of high-amplitude drive levels will have little effect on the maximum operating frequency for drain supply voltages,  $V_{DD}$ , less than about 5 v. However, for higher  $V_{DD}$  levels, high drive levels can increase the maximum frequency significantly.

Current drain is predominantly set by the counters and the driving-signal frequencies. Except at extremely low frequencies, the other on-chip functions will produce only secondary current-drain effects. This results in about the same total drain current value,  $I_{DD}$ , for all members of the family under the same operating conditions. From Figs. 2b and 2c a characteristic plot of  $I_{DD}$  as a function of voltage and frequency can be drawn to determine the current requirements with large-amplitude (rail-to-rail) input signals.

With low-amplitude drive levels (500 mV p-p), the current will remain essentially as shown in Figs. 2b and



**1. Integrated.** The MC145100 family of C-MOS frequency synthesizer chips contain the bulk of the circuitry needed to implement a phase-locked-loop design. Dual-modulus prescaling for higher-frequency operation is optional on three of the family's seven members.

2c for a  $V_{DD}$  of 3 v. For the 5- and 9-v conditions and for operating frequencies in excess of a few hundred kilohertz, higher current drain results.

The reference oscillator and buffer on each chip is used for developing a crystal-controlled reference signal by connecting an external fundamental-mode crystal that is parallel-resonant at the desired operating frequency and by loading the crystal with two capacitors,  $C_{in}$  and  $C_{out}$ , to ground (see Fig. 1 again).

The acceptable loading capacitance,  $C_L$ , seen by the crystal depends upon the oscillator frequency. For a  $V_{DD}$  of 5 v,  $C_L$  should not exceed 32 picofarads for frequencies up to approximately 8 MHz, 20 pF for frequencies in the range of 8 to 15 MHz, and 10 pF for frequencies above 15 MHz.

These guidelines for  $C_L$  take into account IC-capacitance drive capability, variations in stray and IC input/output capacitance, and realistic crystal load-capacitance values. The load capacitance,  $C_L$ , presented across the crystal can be estimated to be a  $C_{in\ total}$  in series with a  $C_{out\ total}$ , where:

$$C_{in\ total} = C_{in} + C_{in\ IC} + C_{in\ stray}$$

$$C_{out\ total} = C_{out} + C_{out\ IC} + C_{out\ stray}$$

with  $C_{in\ IC}$  and  $C_{in\ stray}$  representing the capacitance to ground at  $OSC_{in}$  contributed by the integrated circuit and stray circuit effects, respectively. Similarly,  $C_{out\ IC}$  and  $C_{out\ stray}$  apply to the  $OSC_{out}$  pin.  $C_{in}$  and  $C_{out}$  are capacitors that are added to achieve the proper  $C_L$  value. They should be chosen to make  $C_{in\ total}$  and  $C_{out\ total}$  approximately equal. In practice,  $C_{in}$  and  $C_{out}$  will be

nominally equal. The oscillator can be trimmed to frequency by making a portion or all of  $C_{in}$  variable.

The 145156, -55, and -45 provide a buffered oscillator output,  $REF_{out}$ , for use in other system functions. For the 145152, -51, and -46, the oscillator signal can also be obtained by lightly coupling to  $OSC_{out}$ . This can be done by using a capacitor-tap impedance-transformation network for  $C_{out}$ .

An off-chip reference source can also be used to drive the oscillator input. The reference signal is applied to  $OSC_{in}$  and the crystal, and  $C_{in}$  and  $C_{out}$  are omitted. The oscillator circuitry now behaves as a buffer amplifier. The external reference signal will typically be ac-coupled to  $OSC_{in}$ , but for high-amplitude signals (standard C-MOS logic levels), dc coupling may be used.

**The reference counter's role**

The reference counter divides down the high-frequency reference signal to the desired comparison frequency,  $f_R$ , which is fed into the phase detector. When using the 145156, -55, -52, and -51, the user chooses one of eight possible division values with a 3-bit code applied to division-value select pins  $RA_0$ ,  $RA_1$ , and  $RA_2$ .

The reference counters in the 145146 and -45 are fully user-programmable for integers 3 through 4,096 with a 12-bit binary code. Typically, the desired division value is selected by software through a microprocessor or microcomputer interface with the synthesizer's 4-bit-bus programming structure.

The digital phase-frequency detector on the synthesiz-

