Frequency-divider systems increase flexibility, save parts

A dual-modulus prescaler design provides multiple divide ratios and helps create a 3-chip frequency synthesizer that operates beyond 500 MHz.

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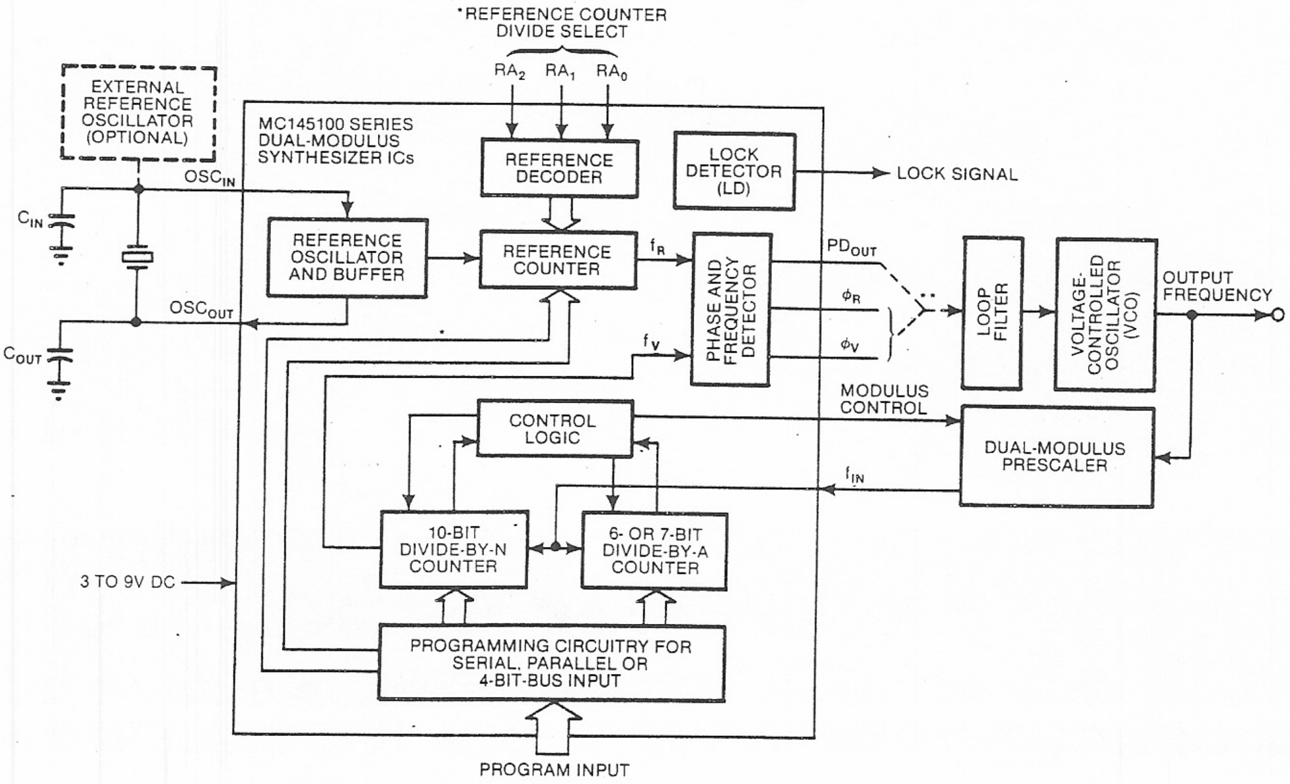
You can increase the divide values of dual-modulus prescaler ICs by using the technique described here. Basically, this technique combines single-chip low-speed programmable counters with the prescaler and an associated binary or decade counter IC (see **box,** "Understanding dual-modulus prescaling"). The programmable counters generate a Modulus Control signal for the prescaler; the counter IC boosts the prescaler's two original divide values to much higher ratios. Increased divide values permit prescaler use with recently introduced CMOS phase-locked-loop (PLL) ICs to form 3-chip frequency-synthesizer systems that



*REFERENCE-COUNTER DIVIDE VALUE SET BY PROGRAM INPUT RATHER THAN BY RA_2, RA_1, AND RA_0 FOR MC145146, -58 AND -59 DEVICES

**CHOICE OF 3-STATE (PD_{OUT}) OR DOUBLE-ENDED ERROR SIGNALS (ϕ_R, ϕ_V) EXCEPT FOR MC145152, WHICH OFFERS ONLY ϕ_R, AND ϕ_V, AND MC145159, WHICH EMPLOYS A SAMPLE/HOLD DETECTOR

Fig 1—Serving as phase-locked-loop frequency synthesizers, *MC145100 Series LSI CMOS devices provide the Modulus Control signal necessary for operation with dual-modulus prescalers. Various prescaler divide values and wide system divide ranges are accommodated. They allow varied programming methods, a choice of 3-state or double-ended error signals and a selection of reference-counter values.*

previously mandated using at least a dozen devices. Moreover, the prescaler can accept input frequencies that exceed 500 MHz.

Although the technique as described uses Motorola parts, you can readily adapt its concepts to similar devices offered by other manufacturers.

Dual division proves better

In practice, dual-modulus prescaling is often used in the design of high-performance PLL frequency synthesizers (**Fig 1**), where the prescaler gets inserted in the loop's feedback path between the voltage-controlled oscillator (VCO) and the low-speed ÷A and ÷N programmable counters. This allows the VCO to operate at high frequencies.

Furthermore, because you can maintain the loop's comparison frequency into the phase and frequency detector at a value corresponding to the desired VCO step size, using a dual-modulus prescaler rather than a fixed single-modulus version results in a marked advantage. With a fixed prescaler, you must decrease the comparison frequency by an amount equal to the prescaling factor to maintain the same VCO step resolution—an undesirable reduction, because it compromises the frequency synthesizer's performance.

Successful dual-modulus prescaling takes advantage of single-chip PLL ICs such as the MC145146, -52, -56, -58 and -59 devices (**Table 1**). These chips furnish the necessary Modulus Control signal and supply most of the required synthesizer functions.

To properly use these chips, however, you must make the prescaler's two divide values (÷P and ÷P+1) large enough to lower the incoming VCO frequency to a value acceptable by the ICs: A 5- to 10-MHz max frequency usually proves adequate. Note that many off-the-shelf high-frequency dual-modulus prescalers possess small

Understanding dual-modulus prescaling

Aimed at frequency-synthesis applications, dual- or 2-modulus prescaling centers on a high-frequency prescaler or divider working in conjunction with low-speed programmable counters.

The combination functions as a programmable counter with a speed equal to that of the prescaler. And because the prescaler divides by only two fixed values, P and P+X, you can design it to operate at higher frequencies than practical with programmable counters. Operation results from configuring the low-speed counters in two sections and employing special decoding/control logic to generate the prescaler's Modulus Control signal, which selects divide value P or P+X in a specific, timed format.

Suppose you designate two low-speed programmable counters as ÷A and ÷N devices. The total system divide value (N_{TOTAL}) therefore becomes a function of P and X plus the value A programmed into the ÷A counter and the value N programmed into the ÷N counter. Typically, you configure the system so that at the beginning of a count sequence, the Modulus Control line goes LOW. This action causes the prescaler to divide by P+X until the ÷A counter counts down from its programmed value, A. During this time, for every P+X pulse into the prescaler's input, the ÷A and ÷N counters both decrement by one. Consequently, after A counts—or (P+X)(A) pulses into the prescaler—the ÷N counter's value is N−A (where N equals the number programmed into the ÷N counter), and the ÷A counter sits at zero.

The system detects this terminal (zero) count and triggers a latch circuit. In turn, that circuit holds the Modulus Control line HIGH and causes the dual-modulus prescaler to start dividing by P. The prescaler continues to divide by P for the remaining N-count sequence—until N−A additional pulses reach the ÷N counter. This condition occurs after (N−A)(P) more prescaler input pulses—corresponding to

$$N_{TOTAL}=(P+X)(A)+(N-A)(P)$$
$$=NP+XA$$

total pulses into the prescaler since the count cycle began.

The ÷N counter then reaches zero, presetting the ÷A and ÷N counters and driving the Modulus Control line LOW. As a result, the prescaler again starts dividing by P+X, and the count cycle repeats. Note that proper dual-modulus prescaling mandates that N must always equal or exceed A—usually not a serious system design constraint.

Fortunately, the total system divide value, $N_{TOTAL}=NP+XA$, can be changed in increments of X as A gets programmed in unit steps. Therefore, by using a prescaler whose divide values equal P and P+1 (ie, making X=1), you can change the total system divide value in steps of one. The defining division equation thus becomes

$$N_{TOTAL}=NP+A,$$

where $N \geq A$.

To cover a range of N_{TOTAL} values in sequence, A must typically equal zero through P−1 in unit steps for a particular N value. The N value then increments to N+1, and the sequence zero through P−1 repeats for A. This procedure continues until the desired N_{TOTAL} range expires. The P value, therefore, dictates the ÷A counter's size; similarly, the maxi-

TABLE 1—MC145100 FREQUENCY-SYNTHESIZER DEVICES

PROGRAMMING METHOD	FEATURES	DEVICE NUMBER	PHASE/FREQ DETECTOR			REFERENCE COUNTER VALUES	LATCHED BAND-SWITCH OUTPUTS	PINS
			3-STATE	DOUBLE-ENDED	SAMPLE/HOLD			
4-BIT DATA BUS	•LATCHES •STROBE/CHIP SELECT •12-BIT PROGRAMMABLE REFERENCE COUNTER	MC145146	YES	YES	NO	3 TO 4096	NO	20
FULLY PARALLEL	•PULL-UPS ON ALL PROGRAMMING LINES •EIGHT REFERENCE COUNTER VALUES	MC145152	NO	YES	NO	8, 64, 128, 256, 512, 1024, 1160 AND 2048	NO	28
SERIAL BIT STREAM	•SHIFT REGISTERS •LATCHES •ENABLE •14-BIT PROGRAMMABLE REFERENCE COUNTER WITH THE MC145158, -59	MC145156	YES	YES	NO	8, 64, 128, 256, 640, 1000, 1024 AND 2048	TWO	20
		MC145158	YES	YES	NO	3 TO 16,384	NO	16
		MC145159	NO	NO	YES	3 TO 16,384	NO	20

mum divide value ($N_{TOTAL\ MAX}$) determines the ÷N counter's size. Thus, the chosen P value, the constraint $N \geq A$ and the ÷A and ÷N counters' ranges set minimum and maximum boundaries on N_{TOTAL}. If $A_{MAX}=P-1$, for example, $N_{MIN} \geq P-1$ yields

$$N_{TOTAL\ MIN}=(P-1)(P)+A_{MIN}$$
$$=(P-1)(P).$$

Moreover,

$$N_{TOTAL\ MAX}=N_{MAX}P+A_{MAX}.$$

Because several P and P+1 choices prove practical, the $N_{TOTAL\ MIN}$ and $N_{TOTAL\ MAX}$ restrictions don't present problems for most applications.

Other considerations in choosing the P value come into play, however. To accommodate the maximum frequency into the prescaler ($f_{IN\ MAX}$), make the P value large enough to meet two conditions:

1. $f_{IN\ MAX}$ divided by P doesn't exceed the ÷A and ÷N programmable counters' frequency capabilities.

2. The period corresponding to the prescaler's output-signal frequency ($f_{IN\ MAX}$ divided by P) must exceed the sum of three times:

- Propagation delay through the dual-modulus prescaler—defined as the time from application of the prescaler's input to the occurrence of an output-signal transition in the direction that triggers the ÷A and ÷N counters (This prescaler output occurs once for each group of P or P+1 input cycles to the prescaler.)
- Prescaler setup or release time relative to the Modulus Control signal
- Propagation time from the input of the ÷A and ÷N counters to the Modulus Control output—the time needed to generate the Modulus Control signal once the ÷A and ÷N counters receive an output-signal edge from the prescaler, corresponding to the completion of a ÷P or ÷P+1 count sequence.

Sometimes the P and P+1 value choices can simplify the code required for prorgramming the ÷A and ÷N counters. Values such as 10/11, 20/21 and 40/41 usually work best when using BCD counters for the ÷A and ÷N functions; values such as 8/9, 32/33, 64/65 and 128/129 work best when employing binary down counters for ÷A and ÷N.

Furthermore, to maximize system frequency capability, the prescaler's output signal (which signifies the completion of each group of P or P+1 input-signal cycles) must make a LOW-to-HIGH transition when using positive-edge-sensitive ÷A and ÷N counters. Similarly, for negative-edge-sensitive counters, the prescaler's output signal must make a HIGH-to-LOW transition to signify the completion of each P or P+1 pulse group. The opposite output phasing—or a delay in the occurrence of the proper output edge transition from the prescaler—subtracts from the amount of time potentially available for the ÷A and ÷N counters and their control-logic function to generate the Modulus Control signal.

Finally, the prescaler must divide by the appropriate value as dictated by the Modulus Control level. Normally, this value equals P when the Modulus Control signal is HIGH and P+1 when the signal is LOW.