Frequency-divider systems increase flexibility, save parts

A dual-modulus prescaler design provides multiple divide ratios and helps create a 3-chip frequency synthesizer that operates beyond 500 MHz.

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You can increase the divide values of dual-modulus prescaler ICs by using the technique described here. Basically, this technique combines single-chip low-speed programmable counters with the prescaler and an associated binary or decade counter IC (see **box,** "Understanding dual-modulus prescaling"). The programmable counters generate a Modulus Control signal for the prescaler; the counter IC boosts the prescaler's two original divide values to much higher ratios. Increased divide values permit prescaler use with recently introduced CMOS phase-locked-loop (PLL) ICs to form 3-chip frequency-synthesizer systems that

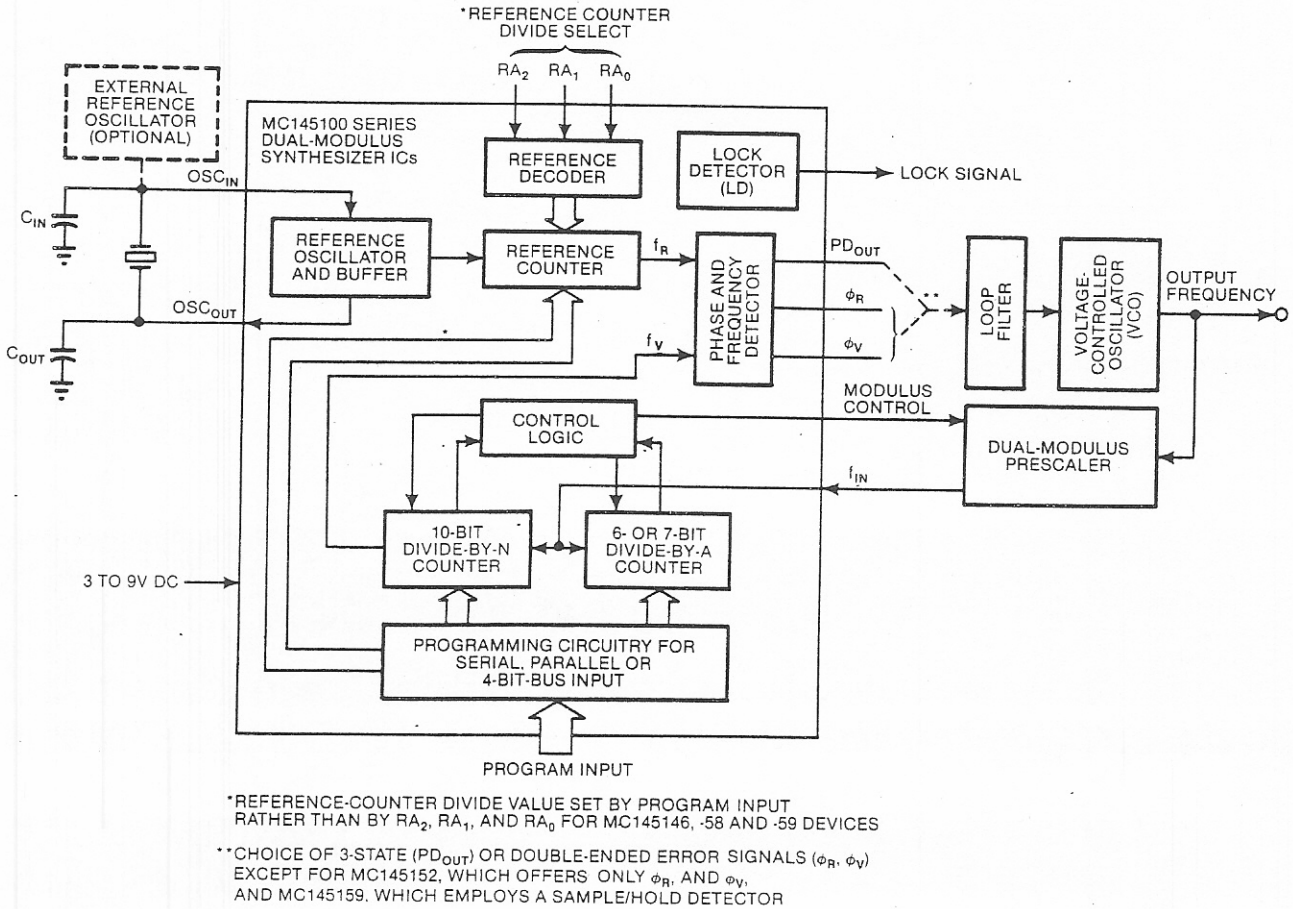


Fig 1—Serving as phase-locked-loop frequency synthesizers, *MC145100 Series LSI CMOS devices provide the Modulus Control signal necessary for operation with dual-modulus prescalers. Various prescaler divide values and wide system divide ranges are accommodated. They allow varied programming methods, a choice of 3-state or double-ended error signals and a selection of reference-counter values.*

Dual-modulus prescalers aid frequency-synthesizer design

previously mandated using at least a dozen devices. Moreover, the prescaler can accept input frequencies that exceed 500 MHz.

Although the technique as described uses Motorola parts, you can readily adapt its concepts to similar devices offered by other manufacturers.

Dual division proves better

In practice, dual-modulus prescaling is often used in the design of high-performance PLL frequency synthesizers (**Fig 1**), where the prescaler gets inserted in the loop's feedback path between the voltage-controlled oscillator (VCO) and the low-speed ÷A and ÷N programmable counters. This allows the VCO to operate at high frequencies.

Furthermore, because you can maintain the loop's comparison frequency into the phase and frequency detector at a value corresponding to the desired VCO step size, using a dual-modulus prescaler rather than a fixed single-modulus version results in a marked advantage. With a fixed prescaler, you must decrease the comparison frequency by an amount equal to the prescaling factor to maintain the same VCO step resolution—an undesirable reduction, because it compromises the frequency synthesizer's performance.

Successful dual-modulus prescaling takes advantage of single-chip PLL ICs such as the MC145146, -52, -56, -58 and -59 devices (**Table 1**). These chips furnish the necessary Modulus Control signal and supply most of the required synthesizer functions.

To properly use these chips, however, you must make the prescaler's two divide values (÷P and ÷P+1) large enough to lower the incoming VCO frequency to a value acceptable by the ICs: A 5- to 10-MHz max frequency usually proves adequate. Note that many off-the-shelf high-frequency dual-modulus prescalers possess small

Understanding dual-modulus prescaling

Aimed at frequency-synthesis applications, dual- or 2-modulus prescaling centers on a high-frequency prescaler or divider working in conjunction with low-speed programmable counters.

The combination functions as a programmable counter with a speed equal to that of the prescaler. And because the prescaler divides by only two fixed values, P and P+X, you can design it to operate at higher frequencies than practical with programmable counters. Operation results from configuring the low-speed counters in two sections and employing special decoding/control logic to generate the prescaler's Modulus Control signal, which selects divide value P or P+X in a specific, timed format.

Suppose you designate two low-speed programmable counters as ÷A and ÷N devices. The total system divide value (N_{TOTAL}) therefore becomes a function of P and X plus the value A programmed into the ÷A counter and the value N programmed into the ÷N counter. Typically, you configure the system so that at the beginning of a count sequence, the Modulus Control line goes LOW. This action causes the prescaler to divide by P+X until the ÷A counter counts down from its programmed value, A. During this time, for every P+X pulse into the prescaler's input, the ÷A and ÷N counters both decrement by one. Consequently, after A counts—or (P+X)(A) pulses into the prescaler—the ÷N counter's value is N−A (where N equals the number programmed into the ÷N counter), and the ÷A counter sits at zero.

The system detects this terminal (zero) count and triggers a latch circuit. In turn, that circuit holds the Modulus Control line HIGH and causes the dual-modulus prescaler to start dividing by P. The prescaler continues to divide by P for the remaining N-count sequence—until N−A additional pulses reach the ÷N counter. This condition occurs after (N−A)(P) more prescaler input pulses—corresponding to

$$N_{TOTAL}=(P+X)(A)+(N-A)(P)$$
$$=NP+XA$$

total pulses into the prescaler since the count cycle began.

The ÷N counter then reaches zero, presetting the ÷A and ÷N counters and driving the Modulus Control line LOW. As a result, the prescaler again starts dividing by P+X, and the count cycle repeats. Note that proper dual-modulus prescaling mandates that N must always equal or exceed A—usually not a serious system design constraint.

Fortunately, the total system divide value, $N_{TOTAL}=NP+XA$, can be changed in increments of X as A gets programmed in unit steps. Therefore, by using a prescaler whose divide values equal P and P+1 (ie, making X=1), you can change the total system divide value in steps of one. The defining division equation thus becomes

$$N_{TOTAL}=NP+A,$$

where $N \geq A$.

To cover a range of N_{TOTAL} values in sequence, A must typically equal zero through P−1 in unit steps for a particular N value. The N value then increments to N+1, and the sequence zero through P−1 repeats for A. This procedure continues until the desired N_{TOTAL} range expires. The P value, therefore, dictates the ÷A counter's size; similarly, the maxi-

TABLE 1—MC145100 FREQUENCY-SYNTHESIZER DEVICES

PROGRAMMING METHOD	FEATURES	DEVICE NUMBER	PHASE/FREQ DETECTOR 3-STATE	PHASE/FREQ DETECTOR DOUBLE-ENDED	PHASE/FREQ DETECTOR SAMPLE/HOLD	REFERENCE COUNTER VALUES	LATCHED BAND-SWITCH OUTPUTS	PINS
4-BIT DATA BUS	•LATCHES •STROBE/CHIP SELECT •12-BIT PROGRAMMABLE REFERENCE COUNTER	MC145146	YES	YES	NO	3 TO 4096	NO	20
FULLY PARALLEL	•PULL-UPS ON ALL PROGRAMMING LINES •EIGHT REFERENCE COUNTER VALUES	MC145152	NO	YES	NO	8, 64, 128, 256, 512, 1024, 1160 AND 2048	NO	28
SERIAL BIT STREAM	•SHIFT REGISTERS •LATCHES •ENABLE •14-BIT PROGRAMMABLE REFERENCE COUNTER WITH THE MC145158, -59	MC145156	YES	YES	NO	8, 64, 128, 256, 640, 1000, 1024 AND 2048	TWO	20
		MC145158	YES	YES	NO	3 TO 16,384	NO	16
		MC145159	NO	NO	YES	3 TO 16,384	NO	20

mum divide value ($N_{TOTAL\ MAX}$) determines the ÷N counter's size. Thus, the chosen P value, the constraint $N \geq A$ and the ÷A and ÷N counters' ranges set minimum and maximum boundaries on $N_{TOT}AL$. If $A_{MAX}=P-1$, for example, $N_{MIN} \geq P-1$ yields

$$N_{TOTAL\ MIN}=(P-1)(P)+A_{MIN}$$
$$=(P-1)(P).$$

Moreover,

$$N_{TOTAL\ MAX}=N_{MAX}P+A_{MAX}.$$

Because several P and P+1 choices prove practical, the $N_{TOTAL\ MIN}$ and $N_{TOTAL\ MAX}$ restrictions don't present problems for most applications.

Other considerations in choosing the P value come into play, however. To accommodate the maximum frequency into the prescaler ($f_{IN\ MAX}$), make the P value large enough to meet two conditions:

1. $f_{IN\ MAX}$ divided by P doesn't exceed the ÷A and ÷N programmable counters' frequency capabilities.

2.The period corresponding to the prescaler's output-signal frequency ($f_{IN\ MAX}$ divided by P) must exceed the sum of three times:

- Propagation delay through the dual-modulus prescaler—defined as the time from application of the prescaler's input to the occurrence of an output-signal transition in the direction that triggers the ÷A and ÷N counters (This prescaler output occurs once for each group of P or P+1 input cycles to the prescaler.)
- Prescaler setup or release time relative to the Modulus Control signal
- Propagation time from the input of the ÷A and ÷N counters to the Modulus Control output—the time needed to generate the Modulus Control signal once the ÷A and ÷N counters receive an output-signal edge from the prescaler, corresponding to the completion of a ÷P or ÷P+1 count sequence.

Sometimes the P and P+1 value choices can simplify the code required for prorgramming the ÷A and ÷N counters. Values such as 10/11, 20/21 and 40/41 usually work best when using BCD counters for the ÷A and ÷N functions; values such as 8/9, 32/33, 64/65 and 128/129 work best when employing binary down counters for ÷A and ÷N.

Furthermore, to maximize system frequency capability, the prescaler's output signal (which signifies the completion of each group of P or P+1 input-signal cycles) must make a LOW-to-HIGH transition when using positive-edge-sensitive ÷A and ÷N counters. Similarly, for negative-edge-sensitive counters, the prescaler's output signal must make a HIGH-to-LOW transition to signify the completion of each P or P+1 pulse group. The opposite output phasing—or a delay in the occurrence of the proper output edge transition from the prescaler—subtracts from the amount of time potentially available for the ÷A and ÷N counters and their control-logic function to generate the Modulus Control signal.

Finally, the prescaler must divide by the appropriate value as dictated by the Modulus Control level. Normally, this value equals P when the Modulus Control signal is HIGH and P+1 when the signal is LOW.

Multiple inputs allow prescalers to offer various divide values

divide values that work ineffectively with the single-chip PLL devices.

To demonstrate how you can increase the divide values of available dual-modulus prescalers such as the ÷5/6 MC12009, the ÷8/9 MC12011 or the ÷10/11 MC12013 (**Table 2**), consider **Fig 2**'s circuit. Each prescaler contains five inputs (E_1 through E_5) that affect the chip's Divide mode (**Fig 3**). The first three (E_1 through E_3) accept ECL levels; the remaining two (E_4 and E_5) require TTL levels. To accommodate level conversion, the ICs contain an ECL-to-TTL translator at pins 4, 5 and 7.

In operation, the MC12011, for example, divides by its lower modulus (÷8) when any one of its E_1 through E_5 inputs is HIGH. It divides by its higher modulus (÷9) when all five input levels are LOW.

To expand these fixed ÷P/P+1 values, you apply a combination of logic levels to the prescaler's E_N inputs so that each divide value repeats a certain number of times before the expanded prescaler system is allowed to generate an output pulse.

For example, to obtain a ÷128 value, the MC12011 must undergo 16 sequences of ÷8 (obtained by driving one or more E_N inputs HIGH) before generating an output pulse. Likewise, to provide a ÷129 value, the MC12011 must trigger 15 sequences of ÷8 (one or more E_N inputs HIGH) plus one sequence of ÷9 (all E_N inputs LOW) before deriving an output pulse.

The system-design problem thus centers on programming the proper E_N input logic levels and controlling output-pulse generation. The solution calls for employing an appropriate counter or flip-flop IC (**Fig 2**'s device B) in conjunction with the dual-modulus device.

TABLE 2—DUAL-MODULUS PRESCALERS' DIVIDE VALUES

DEVICE A (ORIGINAL DIVIDE VALUES)	EXPANDED ÷P/P+1 VALUES	
MC12009 (÷5/6)	80/81*	40/41**
MC12011 (÷8/9)	128/129*	64/65**
MC12013 (÷10/11)	160/161*	80/81**

*CONNECT MC10154 BINARY COUNTER (DEVICE B) AS SHOWN IN FIG 2.
**OMIT CONNECTIONS TO DEVICE A PINS 4 AND 5. DISCONNECT PIN 10 FROM PIN 7 ON DEVICE A AND TIE TO LOW. EXPANDED PRESCALER'S OUTPUT OCCURS AT MC10154 PIN 4.

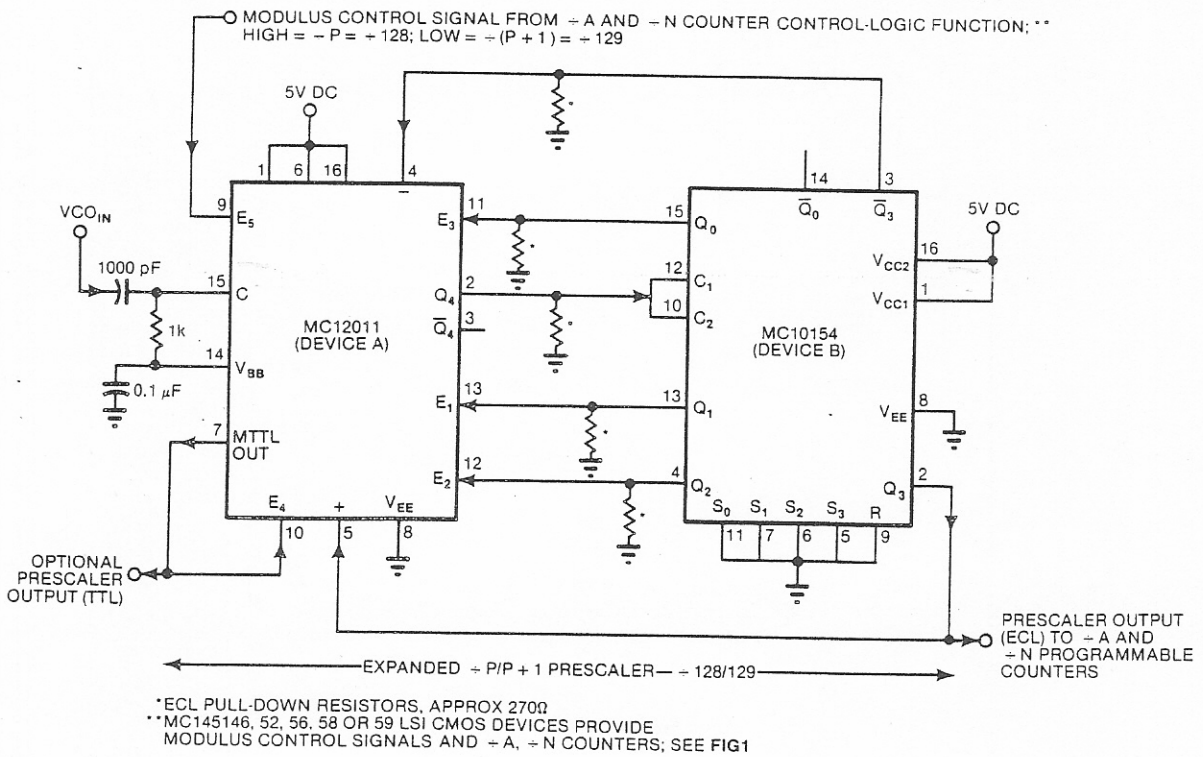


Fig 2—Form an expanded divide-by-128/129 dual-modulus prescaler *by combining an MC10154 binary down counter with an MC12011 ÷8/9 dual-modulus IC. To obtain other divide values, substitute MC12009 or MC12013 prescalers for the MC12011. All ICs provide identical pinouts.*

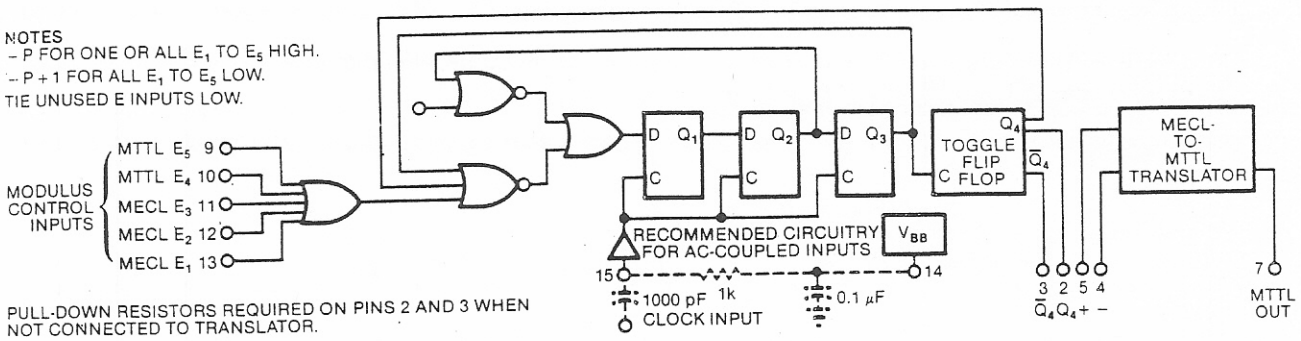


Fig 3—Set up as a high-frequency dual-modulus unit, *the MC12011/12511 ÷8/9 prescaler operates in either of its two divide modes as directed by its five Modulus Control inputs (E_1-E_5). It divides by its lower divide value (÷8) when any one of the five control inputs is HIGH; it divides by the higher divide value (÷9) when all five control inputs are LOW.*

An examination of the truth tables associated with decade (÷10) and binary (÷16) counters' Q outputs shows that you can use some or all of the counters' outputs to keep at least one E_N input HIGH or all inputs LOW for the required number of divide sequences in order to achieve the larger ÷P and ÷P+1 values. Similarly, single and dual flip flops' Q outputs also prove satisfactory.

In each case, connect **Fig 2**'s device A output (Q_4 or $\overline{Q_4}$) to clock the counter (or flip flop). In turn, couple the counter's (or flip flop's) appropriate Q or $\overline{Q}$ outputs to the proper E_N inputs of device A. In addition, always keep one E_N input under the Modulus Control signal's direction, as supplied by the ÷A and ÷N programmable counters, and tie unused E_N inputs LOW. Note that the programmable counters receive their inputs from device B.

For the ICs shown in **Fig 2**, the MC10154's four Q outputs work with ECL levels and the MC12011 furnishes only three such E_N inputs. Thus, use the MC12011's level translator to change the MC10154's Q_3 output to a TTL level. This action results from driving the MC12011 (pins 4 and 5) with MC10154 signals Q_3 and $\overline{Q_3}$. Then, the MC12011's TTL output (pin 7) can drive an available TTL E_N input (for example, E_4).

To achieve other increased divide values, such as ÷80/81 or ÷160/161, substitute a ÷5/6 MC12009 or a ÷10/11 MC12013 IC, respectively, for the ÷8/9 MC12011. Because these three ICs possess equivalent pinouts, you don't have to make any circuit modifications or changes. Accordingly, omitting the connection from MC10154 pin 2 to the prescaler IC and then taking the expanded prescaler's output from MC10154 pin 4 results in ÷40/41 and ÷64/65 values when using the MC12009 and MC12011 prescaler ICs, respectively. In this latter setup, you don't have to use the ECL-to-TTL level translator. Therefore, delete the translator connections and tie E_4 to ground.

When you expand a prescaler's ÷P and ÷P+1 values by the foregoing design technique, the associated counter (device B) must accept the prescaler's (device A) maximum output frequency. Not so obvious effects, though, stem from system phasing and time-delay conditions, which can limit these two devices' operating-frequency range. When phasing is optimum, the signal clocking device B (device A's output) can exhibit a period equal to or greater than the sum of three times: the propagation time through device A, device A's setup or release time relative to its E_N inputs and B's propagation time to its first output.

Optimum system phasing allows the ÷A and ÷N programmable counters and their counter-control logic function the maximum time to generate the Modulus Control signal. The actual time available equals device B's output signal period minus device A's propagation and setup or release times, relative to its E_N inputs, and minus device B's propagation time to its output signal edge, which drives the ÷A and ÷N programmable counters. With positive-edge-triggered ÷A and ÷N counters such as those provided by the MC145146 through MC145159 ICs, optimum system phasing occurs only when you employ only the Q outputs (as opposed to the $\overline{Q}$ outputs) of a positive-edge-triggered down counter, such as the MC10154 IC, for device A's E_N inputs.

When you must use other counter types for device B, carefully study the system's timing constraints to determine which counter output (Q or $\overline{Q}$) results in optimum timing for a particular application. For example, if you utilize the MC10178 binary up counter for device B, use the $\overline{Q_0}$ rather than the Q_0 output to drive the E_3 input for optimum prescaler frequency capability. In addition, when using the MC10178, the time available for generating the Modulus Control signal proves shorter by half. The time reduction results because Q_3's positive-going edge, which indicates the end of a ÷P or ÷P+1 count sequence, gets delayed by approximately half of an output-signal

Low-speed programmable counters generate Modulus Control signals

period. Although this delay penalty appears severe, you could tolerate it when the system functions with large prescaling factors such as ÷128/129. Under these conditions and depending on input-frequency requirements, sufficient output-signal time would likely remain for generating Modulus Control.

Extension of the prescaling design technique can yield still other ÷P and ÷P+1 values when using different counter or flip-flop ICs for device B. For example, a biquinary (a mixed-based notation in which the leading digit of each digit pair is in binary format and the trailing digit is base 5) decade counter's ÷5 and ÷10 functions can furnish ÷25/26, ÷40/41, ÷50/51, ÷80/81 and ÷100/101 values. And a dual flop flop can similarly provide ÷20/21, ÷32/33 and ÷40/41 values.

Take advantage of LSI IC benefits

To execute the ÷A and ÷N programmable functions, the MC145146 through MC145159 ICs employ positive-edge-triggered binary down counters. Their ÷N counters contain 10 bits; the ÷A counters, seven bits. (The MC145152 contains a 6-bit ÷A counter.)

When powered from 5V dc, these ICs generate the Modulus Control signal in 50 nsec typ (100 nsec worst c[illegible]) after receiving the prescaler's particular positive-going-edge output that corresponds to the completion of a ÷P or ÷P+1 count sequence. Further, when powered from 5V dc and operating with a 5-MHz input to the ÷A and ÷N programmable counters and a 10-MHz signal into the reference counter, the ICs draw only 3 mA. They require even less current at lower input frequencies.

Except for their programming method, the ICs have similar characteristics (**Table 3**). The 4-bit-data-bus and serial-bit-stream-programmed units suit interfacing with μC- and μP-based controllers. The MC145146, MC145158 and MC145159 ICs allow you to control the reference counter as well as the ÷A and ÷N counters via their program structure. This capability permits changing the reference divide value in unity steps. The MC145152 and MC145156 ICs let you choose one of eight divide values for the reference counter by driving their RA_0, RA_1 and RA_2 inputs.

Other PLL ICs, such as the MC145145 (4-bit data bus), MC145151 (parallel) and MC145155 and MC145157 (serial), provide similar functions but omit the Modulus Control generation and ÷A-counter capabilities. These ICs come with 14-bit ÷N counters for servicing nondual-modulus-prescaler designs. You can program their ÷N counters for values of 3 through 16,384. EDN

TABLE 3—MC145146 LSI DEVICES' CHARACTERISTICS

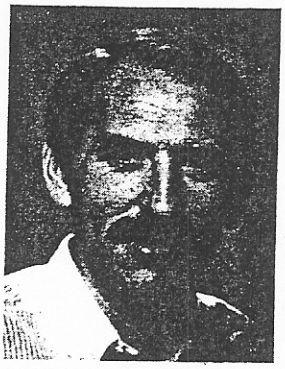
OPERATING VOLTAGE	3 TO 9V DC
TYPICAL CURRENT DRAIN WITH F_{IN} = 5 MHz, OSC_{IN} = 10 MHz AND V_{DD} = 5V, AT 25 °C	3 mA DC
OPERATING TEMPERATURE	−40 TO +85 °C
MAXIMUM F_{IN} with 500 mV PEAK-TO-PEAK SINE WAVE AND V_{DD} = 5V	15 MHz MIN
SYSTEM FREQUENCY WITH DUAL-MODULUS PRESCALER	TO >500 MHz
DUAL-MODULUS PRESCALER RANGE	
MC145146, 56, 58, 59	DIVIDE BY 3/4 THROUGH 128/129,
MC145152	DIVIDE BY 3/4 THROUGH 64/65
MAXIMUM TOTAL DIVISION VALUE (N_{TOTAL}) WITH DUAL-MODULUS PRESCALING	
MC145146, 56, 58, 59	131,199
MC145152	65,599
[illegible]E REQUIRED TO GENERATE MODULUS CONTROL SIGNAL AT 25 °C, WITH V_{DD} = 5V	50 nSEC TYP 100 nSEC MAX

References

1. Motorola Semiconductor Products Sector, *The Technique of Direct Programming by Using a Two-Modulus Prescaler,* Application Note AN-827, Phoenix, AZ, 1981.

2. Nichols, J, and Shinn, C, "Pulse Swallowing," *EDN,* October 1, 1970, pgs 39-42.

Author's biography



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