RF Modems — Part II

Part I provided an introduction to the subject of RF modems along with a description of useful ICs. Designs for single channel units were also presented. Part II covers various multiple channel (frequency agile) modem designs.

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Multiple Channel (Frequency Agile) Modems

Frequency agile modems are described under two categories. "Fully frequency agile" and "paired channels." Either modem type can be programmed at will for operation on any one of many possible channels. The term "fully frequency agile" is being reserved for modems that are capable of having their transmitters and receivers programmed independent of each other. This allows the transmit/receive frequency separation or offset to be varied. The term "paired channels" is being used to describe modems whose transmit and receive frequencies have a built-in separation which remains constant as the modem is programmed to different channels (channel pairs).

Fully Frequency Agile Modem

One implementation of a fully frequency agile modem is described by the block diagram in Figure 1 and the schematic diagram in Figure 2. Nominal performance data and other characteristics of the modem are given in Table 1 and various modem signal frequencies and synthe-

Table 1
Summary of Characteristics for the Fully Frequency Agile RF Modem Described in Figures 1 and 2

	General
Type:	Fully frequency agile
Maximum Data Rate:	125 Kbps modem (limited by digital interface circuits to 50 Kbps)
Modulation:	FSK
Number of Channels:	Eleven as shown, but the limit is set by the transmit filter bandwidth employed. The number of channels can be extended to approximately 32 with an appropriate filter. The maximum useful bandwidth is dictated by the lowest injection frequency (10.2 MHz) to the transmit mixer.
Channel Spacing:	Three times deviation or 300 KHz
Transmitter Output Level:	-6 dBmv to +30 dBmv (adjustable)
RF Terminal Impedance:	75 ohms nominal (in band)
Transmit On/Off Ratio:	>80 dB
RTS Delay:	≤5 microseconds
Receiver IF Frequency:	10.7 MHz (center frequency
Reciever IF Bandwidth:	±75 KHz nominal
DCD Delay:	≤5 microseconds
Power Requirements:	$+5V_{DC}$, $+12V_{DC}$, GND
	Digital Interface Lines
D_0 — D_7:	Channel control data and address inputs for the transmit and receive PLL frequency synthesizers. Also, the ACIA data input and output.
A_0, A_4, SCS, E:	Address and clock input to the ACIA
A_1, E, SCS:	Strobe input for the transmitter PLL
A_2, E, SCS:	Strobe input for the receiver PLL)
Q:	Transmit and receive clock input
Cart:	Interrupt request output to the computer
R/W:	Read/Write input into the ACIA from the computer