RF Modems — Part II

Part I provided an introduction to the subject of RF modems along with a description of useful ICs. Designs for single channel units were also presented. Part II covers various multiple channel (frequency agile) modem designs.

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Multiple Channel (Frequency Agile) Modems

Frequency agile modems are described under two categories. "Fully frequency agile" and "paired channels." Either modem type can be programmed at will for operation on any one of many possible channels. The term "fully frequency agile" is being reserved for modems that are capable of having their transmitters and receivers programmed independent of each other. This allows the transmit/receive frequency separation or offset to be varied. The term "paired channels" is being used to describe modems whose transmit and receive frequencies have a built-in separation which remains constant as the modem is programmed to different channels (channel pairs).

Fully Frequency Agile Modem

One implementation of a fully frequency agile modem is described by the block diagram in Figure 1 and the schematic diagram in Figure 2. Nominal performance data and other characteristics of the modem are given in Table 1 and various modem signal frequencies and synthe-

Table 1
Summary of Characteristics for the Fully Frequency Agile RF Modem Described in Figures 1 and 2

	General
Type:	Fully frequency agile
Maximum Data Rate:	125 Kbps modem (limited by digital interface circuits to 50 Kbps)
Modulation:	FSK
Number of Channels:	Eleven as shown, but the limit is set by the transmit filter bandwidth employed. The number of channels can be extended to approximately 32 with an appropriate filter. The maximum useful bandwidth is dictated by the lowest injection frequency (10.2 MHz) to the transmit mixer.
Channel Spacing:	Three times deviation or 300 KHz
Transmitter Output Level:	-6 dBmv to +30 dBmv (adjustable)
RF Terminal Impedance:	75 ohms nominal (in band)
Transmit On/Off Ratio:	>80 dB
RTS Delay:	≤5 microseconds
Receiver IF Frequency:	10.7 MHz (center frequency
Reciever IF Bandwidth:	±75 KHz nominal
DCD Delay:	≤5 microseconds
Power Requirements:	$+5V_{DC}$, $+12V_{DC}$, GND
	Digital Interface Lines
D_0 — D_7:	Channel control data and address inputs for the transmit and receive PLL frequency synthesizers. Also, the ACIA data input and output.
A_0, A_4, SCS, E:	Address and clock input to the ACIA
A_1, E, SCS:	Strobe input for the transmitter PLL
A_2, E, SCS:	Strobe input for the receiver PLL)
Q:	Transmit and receive clock input
Cart:	Interrupt request output to the computer
R/W:	Read/Write input into the ACIA from the computer

sizer programming information are summarized in Table 2. (Keep in mind that the transmitter and receiver can be programmed independent of each other i.e. one may choose to have the modem transmit on channel one and receive on channel five, etc.)

One may observe from Figures 1 and 2 that the modem consists of four major sections (not counting the MC6850 Asynchronous Communications Interface Adapter, ACIA, since it is common for this function to be considered as part of the digital interface system rather than the modem itself):

- Transmitter Phase-Locked-Loop (PLL) Frequency Synthesizer
- FSK Transmitter
- FSK Data Receiver
- Receiver PLL Frequency Synthesizer

The transmitter frequency synthesizer generates an error signal which is filtered and amplified by the loop filter and becomes a control voltage for the transmitter VCO. The error signal and thus the VCO's frequency is a function of the digital programming information provided to the MC145145 PLL IC. This information is under control of software and may be altered to fit particular application requirements. Since the 145145 is specified for operation to 15 MHz max. At $5V_{DC}$ (-40°C to +85°C) a prescaler is used to reduce the VCO's frequency to acceptable values. Although smaller divide values could be used, the divide-by-20 MC3396 prescaler provides a good solution which is both low cost and in a compact eight pin package. The receiver frequency synthesizer is of like design and controls the receiver's VCO which provides the injection signal for the receiver mixer. Both the receiver oscillator and mixer are part of the MC3356 data receiver IC.

The transmitter and receiver synthesizers are independently programmed via their data (D_0, D_1, D_2, D_3) and address (A_0, A_1, A_2) input lines. These lines (and also the MC6850's data inputs) share a common data bus. The appropriate IC is selected by its strobe (ST) or chip select (CS2) input signal. Other single chip PLL synthesizer choices exist in the MC14145 family and could be used rather than the MC145145 devices. The other family members differ from the MC145145 primarily in the method used for channel programming. For example, the MC145155 or 57 employ a serial data stream and the MC145151 requires fourteen parallel data bits.

The transmitter section consists of the PLL controlled high frequency transmitter VCP and a lower frequency (nominally 10.2 MHz) oscillator. The transmit VCO determines the desired transmit channel and provides frequency stability since it is locked to the 10.24 MHz crystal reference oscillator housed in the transmitter PLL IC. A ceramic resonator adds stability to the lower frequency oscillator yet allows it to be frequency shift keyed or modulated by the serial data bit stream (MC6850 T_X data output). The two oscillator signals are applied to the transmitter mixer. The mixer's difference frequency product is allowed to pass through the transmitter's output filters/amplifiers and becomes the FSK transmit signal. Both oscillators and the mixer are provided by the MC1374 IC. To minimize start-up time, both transmitter oscillators run continuously. The transmit output signal, however, is inhibited when desired by taking the RTS (Ready to Send) line high which causes the transmit mixer and output amplifiers to be biased off.

The band of channels the transmitter can be made to operate over is primarily dictated by its output filters. Standard 45 MHz TV IF SAW filters are being used and this unnecessarily restricts the trans-

Table 2
Signal Frequencies and Channel Programming Information for the Modem Described in Figures 1 and 2

Channel Number	Channel Center (MHz)	Rcvr VCO Freq (MHz)	Trans VCO Freq (MHz)	Trans PLL ÷ N (Note 1)	Rcvr PLL ÷ N (Note 1)
0	42.5	53.2	52.7	527	532
1	42.8	53.5	53.0	530	535
2	43.1	53.8	53.3	533	538
3	43.4	54.1	53.6	536	541
4	43.7	54.4	53.9	539	544
5	44.0	54.7	54.2	542	547
6	44.3	55.0	54.5	545	550
7	44.6	55.3	54.8	548	553
8	44.9	55.6	55.1	551	556
9	45.2	55.9	55.4	554	559
10	45.5	56.2	55.7	557	562

Notes:

1. Trans $\div N = \frac{\text{Trans VCO}}{(P)(f_R)}$; Rcvr $\div N = \frac{\text{Rcvr VCO}}{(P)(f_R)}$

Where:
P = PLL Prescaler Divide Value = 20

f_R = Phase Detector Comparison Freq = $\frac{10.24\ \text{MHz}}{\text{Ref Divider}} = \frac{10.24\ \text{MHz}}{2048} = 5\ \text{KHz}$

2. Trans VCO = Channel Freq + 10.2 MHz

3. Rcvr VCO = Channel Freq + Rcvr IF = Channel Freq + 10.7 MHz

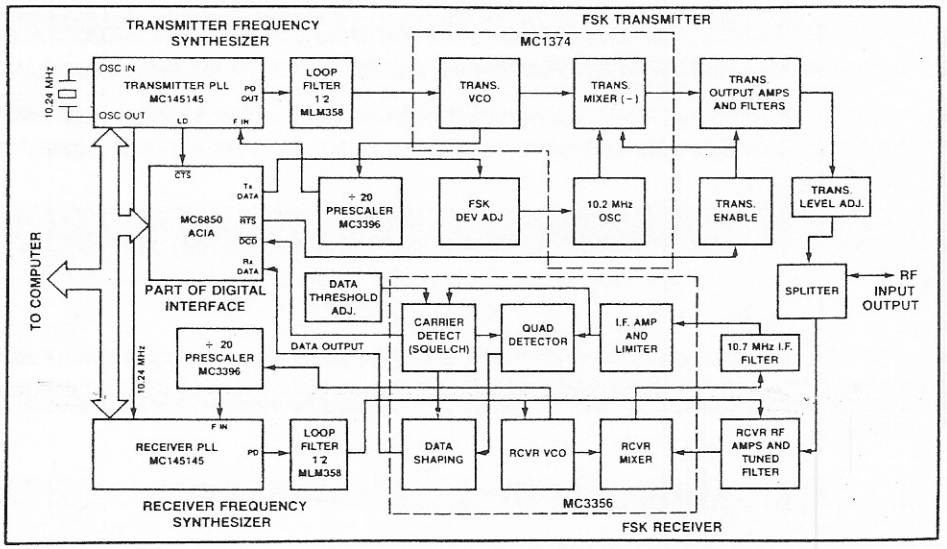


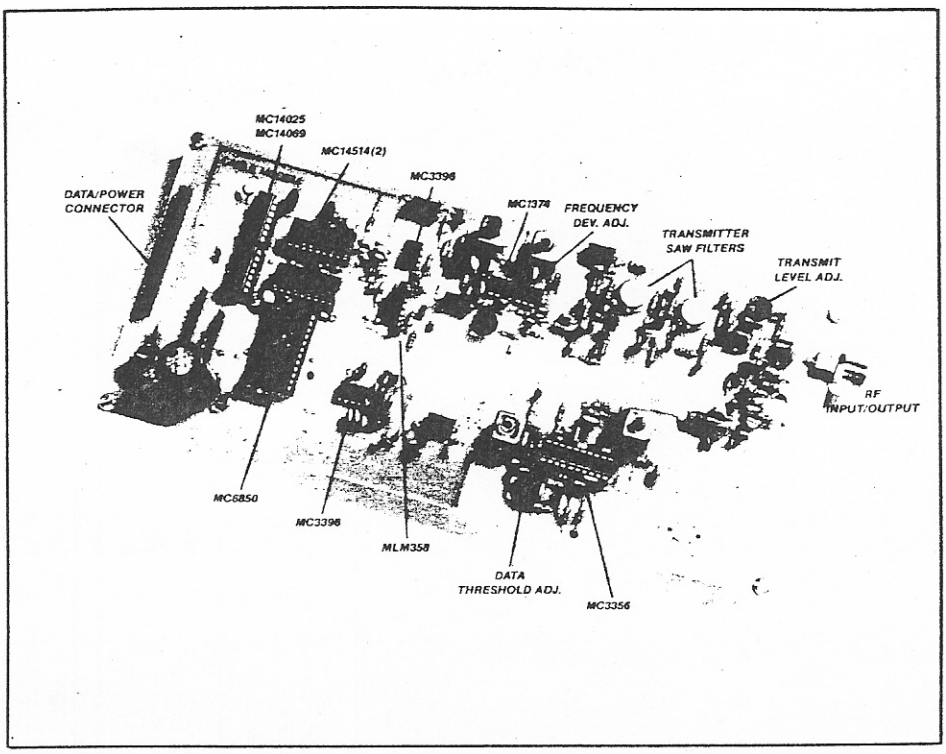
FIGURE 1. Fully frequency agile RF modem block diagram.

mitter's total bandwidth to approximately 3 MHz.

The MC3356 data receiver IC preceded by a discrete RF amplifier and a varactor tuned filter stage make up the modem's receiver section. The filter is tuned by the same synthesizer error voltage that controls the receiver's VCO. The receiver's VCO is tuned such that only the incoming RF channel to be received is converted to the receiver's IF passband and allowed to pass through the 10.7 MHz IF filter. The IF filter used is a standard product manufactured for FM broadcast receiver applications. Other IF values and filters of various bandwidths can also be used with the 3356.

The modem just described can, within limits, be modified to serve different performance requirements. For example:

- Using a wider bandwidth filter for the receiver IF will allow the MC3356 to receive higher data rates. Higher data rates will, of course, also require the RF channel spacings to increase and thus the number of channels possible in a given system bandwidth allocation decreases.
- Using transmitter output filters having different passbands will allow other channel frequencies to be generated. Also, the use of wider bandwidth filters



Photograph of fully frequency agile RF modem employing the MC3356 data receiver IC and described in Figures 1 and 2.

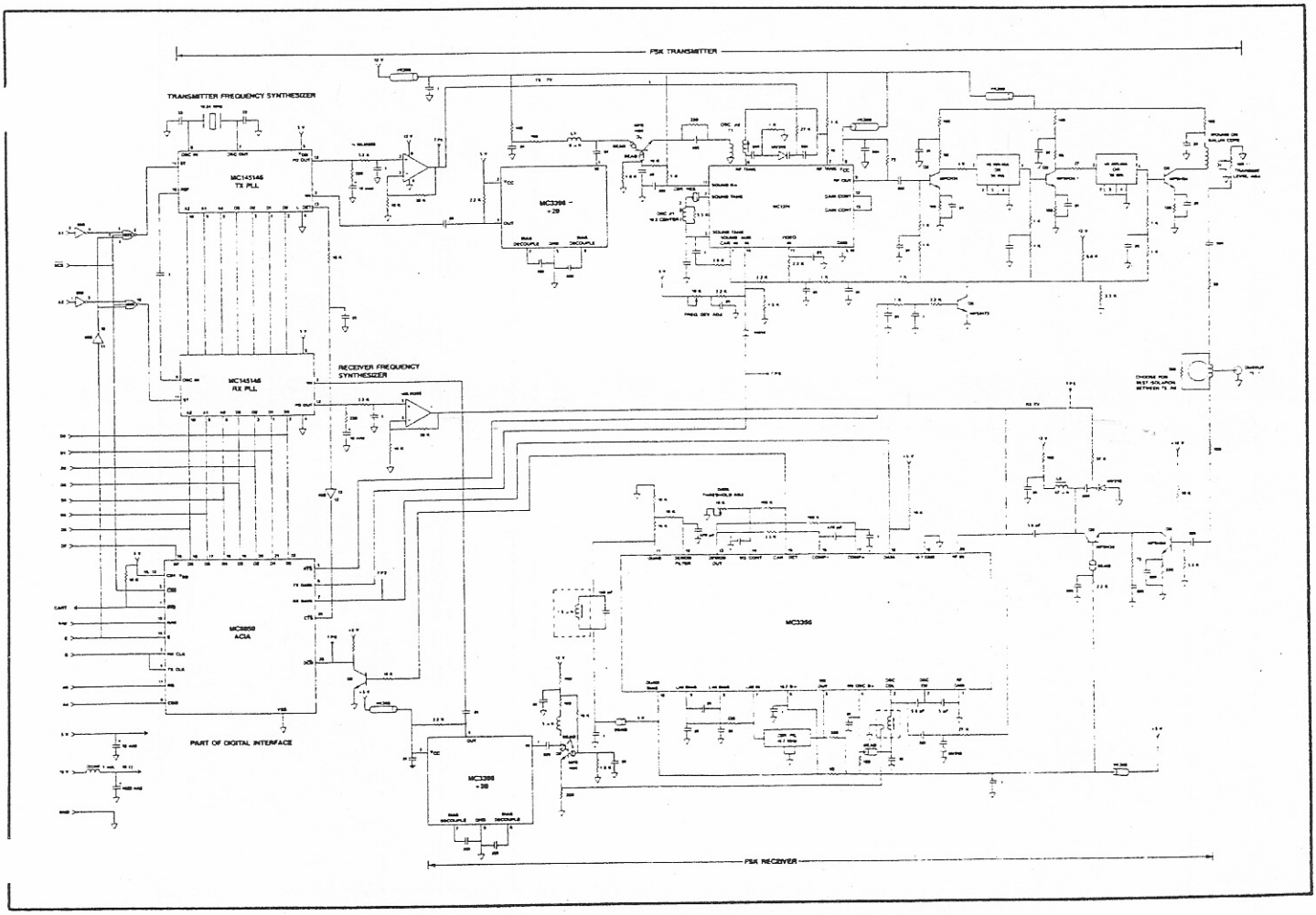


FIGURE 2. Fully frequency agile RF modem schematic.

will permit channels to be spaced over a wider frequency range.

- Modifications of only the software will allow different data rates, system protocols, channel spacings, and channel frequency values to be achieved (within limits of the hardware).

Frequency Agile Paired Channel Modems

Figures 3, 4 and 5 describe a design concept that can be used to achieve frequency agile paired channel modems having a variety of data rates and channel spacings. In each case the basic approach is tailored to accomplish the proper FSK transmitter carrier shift to optimize spectrum bandwidth requirements — consistent with the maximum data rate. Although shown as paired channel designs, the modems can also be turned into fully frequency agile systems with the addition of another frequency synthesizer loop. By way of example, this has been done for the modem described in Figure 3 (see Figure 7).

Inputs and outputs for the paired channel modems of Figures 2, 4, and 5 are defined as follows:

Inputs

Power: $+5V_{DC}$, $+12V_{DC}$

T_X Data: Serial data (NRZ) used to FSK modulate the transmitter's VCO.

RTS: Read to Send signal. Its logic level is used to enable/disable the transmitter's RF output.

RF Input: FSK modulated input signal for the receiver.

Prog/ Channel Select Lines: Digital input code used for programming the PLL frequency synthesizer. Selects modem's operating channel pair. In the case of Figure 5, programming can be accomplished using mechanical switches, as indicated, to program the MC145151 synthesizer IC.

Outputs

RF Output: Transmitter output (FSK modulated carrier).

DCO: Data carrier detect. High in the presence of a received carrier.

R_X Data: Received data obtained by demodulation of the received FSK RF input signal.

T_X Clock: The FSK PLL modulus control line. It is used to synchronize T_X Data to prevent the synthesizer counters from being reloaded during bit transitions.

Except for Figure 4, the paired channel approaches maintain the receiver channel frequencies within range of the MC3356 data receiver IC. The modem in Figure 4 is configured to employ a transmit/receive offset of 192.250 MHz (with low side transmit) and therefore requires RF input frequencies which are out of range of the 3356. The 192.250 MHz offset is one of the standards for Local Area Networks (LANs). As indicated, a wide band front end (RF unit) is employed to lower the incoming channels to a frequency value acceptable to the 3356. The RF unit can be similar in design to existing CATV converters.

In establishing operating frequency ranges for the modems, consideration must be given to the location of receiver image and half IF spurs and their impact on the receiver's front end filter requirements. Also, consistent with conserving system bandwidth, all the design approaches employ a suitable bandpass filter prior to the transmitter's doubly balanced mixer. This filter limits the FSK modulation sideband energy to a restricted bandwidth appropriate for the channel separations employed. Note that the

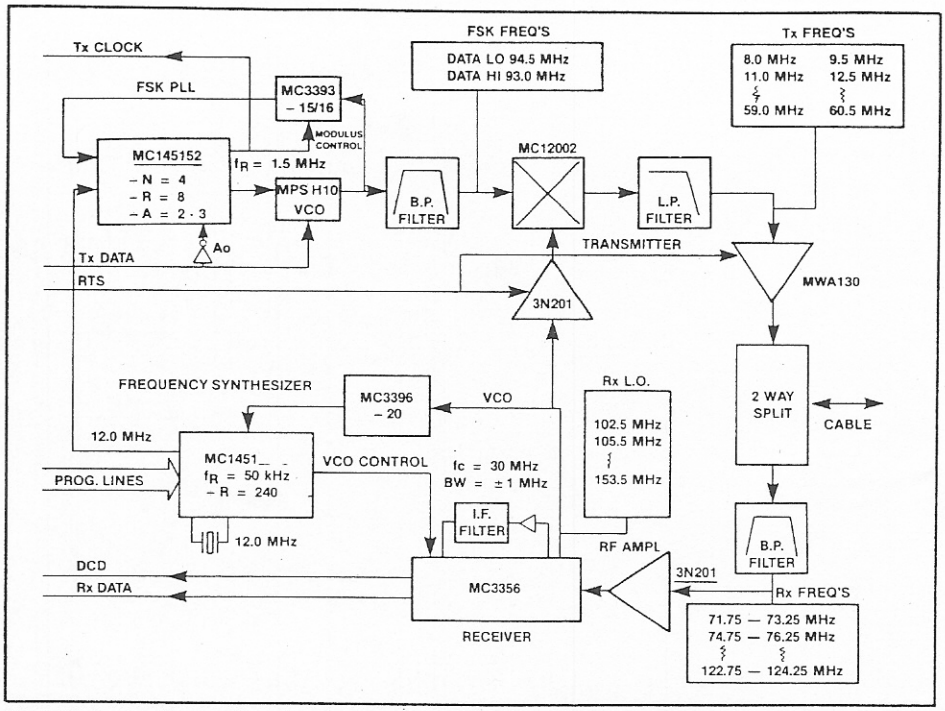


FIGURE 3. Paired 18 channel modem, with 63.75 MHz offset, 1.5 Mbps/channel.

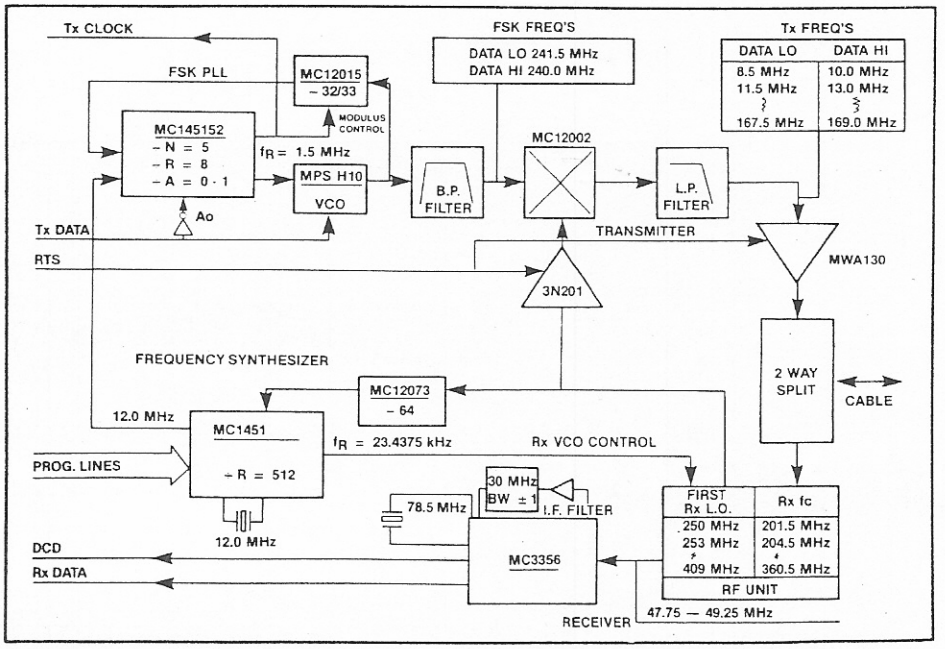


FIGURE 4. Paired 54 channel modem with 192.25 MHz offset, 1.5 Mbps/channel.

FSK signal frequency into the mixer does not have to change for different operating channels. This allows a fixed bandpass filter to be used.

A single frequency synthesizer provides for both transmit and receive channel control. The synthesizer uses one MC145XX family IC chosen for the desired programming interface and one fixed value prescaler. The synthesizer controls the receiver's local oscillator. In addition to providing receiver mixer injection, this oscillator signal is also buffered and applied to the transmitter's mixer. The second input to the transmit mixer is the FSK signal. The mixer's difference frequency product is passed by the low pass transmitter output filter and becomes the FSK transmit channel carrier.

The method used to generate the FSK signal is the key to achieving high frequency accuracy on a signal that can also be FSK modulated with NRZ data. A unique PLL approach (labeled FSK PLL in the figures) is employed where both the PLL VCO and one bit (A_0) in the PLL's programmable divider are modulated by the data to be transmitted (T_XData). This is accomplished in the examples by using a dual-modulus prescaling technique and requires a phase detector comparison frequency (f_R) in hertz which is equal to or an integer times the data rate in bits per second. For example, the modem in Figure 3 which employs a phase detector comparison frequency, f_R, of 1.5 MHz can also transmit data rates of ½, ⅓, ¼, etc. times the 1.5 Mbps data rate indicated i.e. data rates of 750, 500, 375 Kbps. Other data rates require different f_R frequencies. Flexibility of obtaining different f_R values is provided by the MC145XX family of ICs. It is not necessary to program the FSK PLL for different operating channels. The MC145152 device is best suited for the application since it is capable of controlling a variety of dual-modulus prescalers and also of providing direct access to the proper counter bit that must be modulated by the data to be transmitted.

The modem shown in Figure 5 is similar to the modems in Figures 3 and 4 except that the channel control frequency synthesizer is intended to be programmed via mechanical switch settings rather than from a microcomputer/microprocessor program input. The fully parallel programmable MC145151 IC has been used to accomplish this.

Low Cost Half-Duplex Modem

A unique case exists when a paired channel modem's offset frequency is equal to zero. When this occurs, the transmit and receive channel frequencies become identical and full-duplex operation is no longer possible. However, half-duplex performance is accommodated and, for certain specifications, achieved very economically. Such a low cost design is depicted in Figure 6. It employs a modification of the PLL approach described in Figures 3, 4 and 5 for generating the FSK transmit signal but, since transmission and reception are not allowed simultaneously, the same PLL and VCO is also used to provide the necessary transmit and receive frequencies for each channel. The transmit signal is generated directly from the MC3356 receiver's local oscillator (VCO) by causing the oscillator to be slewed to the transmit frequency by the PLL. The amount of VCO slewing required between transmit/receive is equal to the receiver's IF. The modem's transmit/receive frequencies are chosen to linearize the VCO's voltage to frequency transfer characteristic while maximizing the number of channels available and minimizing the number of lines required for channel control.

Note that during receive, the receiver's local oscillator (VCO) can be one of two frequencies for each channel — determined by the T_X Data input being disabled "high" or "low." This would result in one of two values for the receiver's IF center frequency, either 10.65 MHz or 10.75 MHz. A network system using the modem should be defined to cause T_X

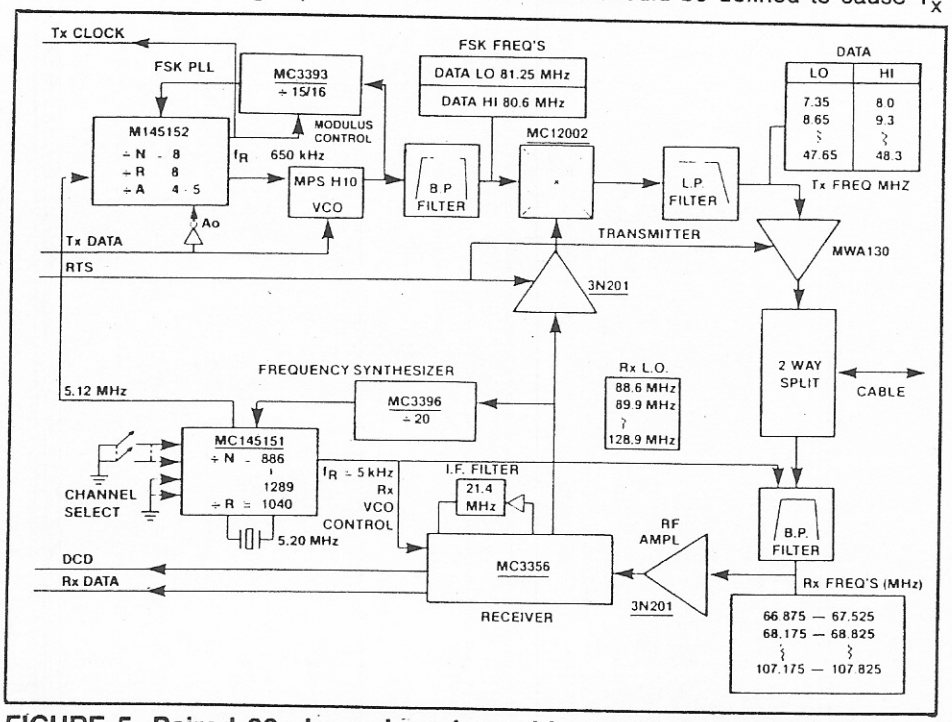


FIGURE 5. Paired 32 channel modem with manual programming and 59.525 MHz offset, 650 Kbps/channel.

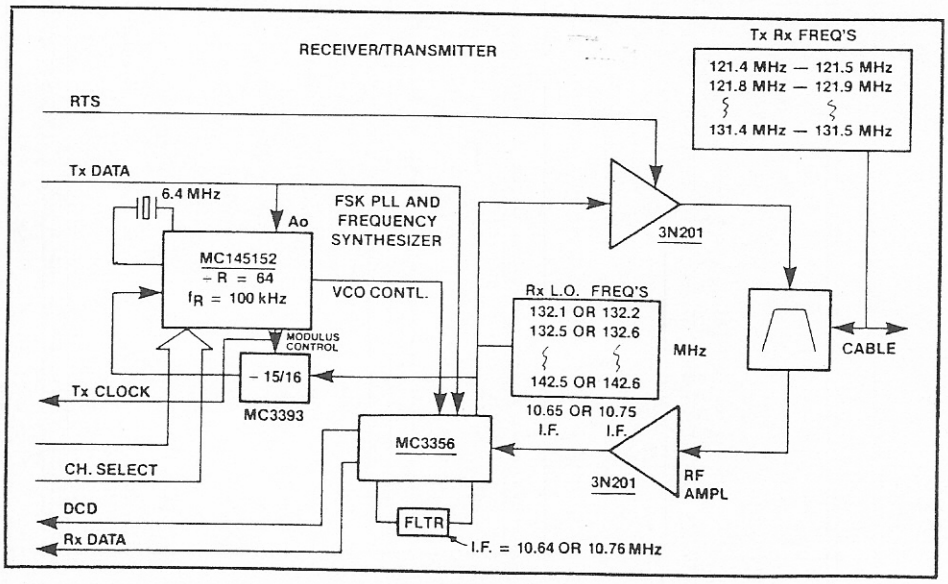


FIGURE 6. 28 channel, low cost half duplex modem, 100 Kbps/channel.

Data to always be disabled to the same level (either consistently high or consistently low) when in the receive mode. This prevents the IF filter from having to accommodate two different IF center frequencies.

High Data Rate Fully Frequency Agile Modems

Each of the paired channel modems presented in Figures 3, 4 and 5 can be converted into fully frequency agile designs by incorporating an additional PLL frequency synthesizer and associated VCO. This new synthesizer is used to provide the transmitter mixer's injection signal. This mixer signal is from the receiver's local oscillator in the noted paired channel designs. As an example of this technique, the 1.5 Mbit paired channel modem of Figure 3 has been converted into a fully frequency agile design by incorporating the additional PLL — see Figure7.

The key difference between the full frequency agile design in Figure 7 and the design in Figure 1 lies with the method used to generate the FSK transmit signal. Figure 7 employs the PLL approach described for the paired channel designs where both the PLL VCO and a single bit in the PLL's programmable divider are modulated by the data to be transmitted. This allows the greater frequency deviation required for the higher data rates and still maintains high carrier frequency accuracy. The approach also allows a wide carrier frequency operating range.

Another approach for high data rate (to approximately 500 Kbps) fully frequency agile modems is to provide the injection signal for the transmitter's mixer from a fixed frequency oscillator and change the transmit channel frequency by programming the same PLL that generates the FSK signal — see Figure 8. This system is described for a data rate of 500 Kbps per channel but can be modified for lower data rates e.g. 50, 100, or 200 Kbps which will allow the use of a low cost 10.7 MHz ceramic filter in the receiver's IF section. However, with the approach in Figure 8, the channel spacing and thus the system bandwidth required for a given data rate is greater than is necessary with the method described in Figure7. This occurs for two reasons:

- The FSK signal of Figure 8 is not passed through a bandpass filter to remove the unnecessary modulation sidebands before the signal is applied to the transmit mixer. The use of a bandpass filter is not desirable with this approach since it would have to be electronically tuned in conjunction with the transmitter's channel changes.
- The PLL method being used to generate the FSK signals limits the loop's VCO tuning interval (and thus the transmitter's channel spacings) to even integers of the frequency deviation. Without the bandpass filter discussed above, channel spacings of two times the deviation do not allow reliable adjacent channel performance because of overlapping modulation sidebands. Four times the deviation then becomes the minimum channel spacing.

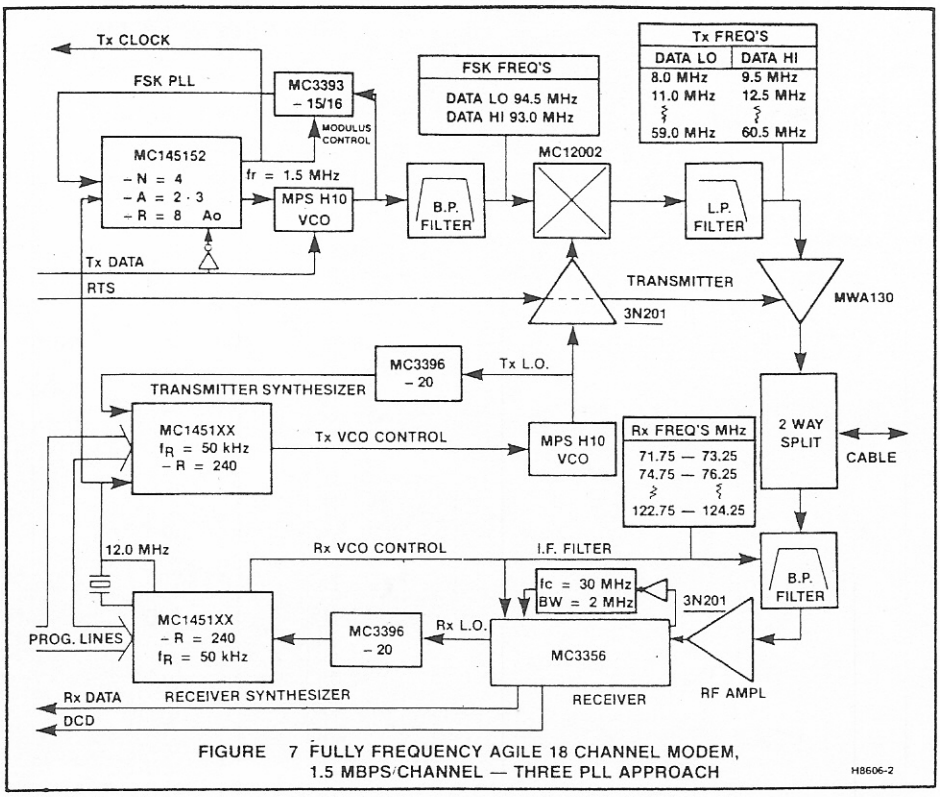


FIGURE 7 FULLY FREQUENCY AGILE 18 CHANNEL MODEM, 1.5 MBPS/CHANNEL — THREE PLL APPROACH

H8606-2

FIGURE 7. Fully frequency agile 18 channel modem, 1.5 Mbps/channel — three PLL approach.

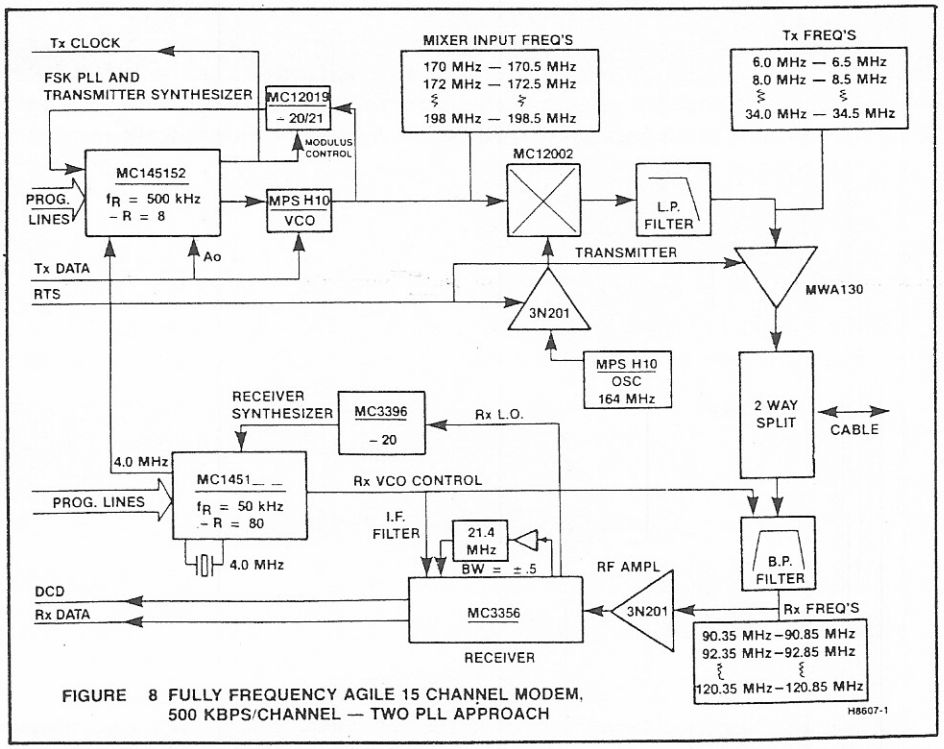


FIGURE 8 FULLY FREQUENCY AGILE 15 CHANNEL MODEM, 500 KBPS/CHANNEL — TWO PLL APPROACH

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FIGURE 8. Fully frequency agile 15 channel modem, 500 Kbps/channel — two PLL approach.