MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN968

A Digital Voice/Data Telephone Set

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OVERVIEW

This application note presents the design of a digital voice/data telephone set which provides standard analog telephone functions while simultaneously transmitting 9600 baud asynchronous data. This telephone set is built around Motorola's MC145422/26 UDLT (universal digital loop transceiver) family of voice/data ICs. The UDLTs provide 80 kbps full-duplex synchronous communication at distances of up to two kilometers on a single 26 AWG twisted pair telephone wire. The MC14403 codec/filter and MC145428 data set interface (DSI) convert voice and data signals respectively into digital formats compatible with the UDLTs' transmission scheme. The design includes the MC145413, a full-featured pulse/tone dialer, and the MC145406, a CMOS RS-232 driver/receiver for communicating with an external terminal or PC. An efficient switching power supply utilizing the MC34129 provides isolated power for the digital telephone set directly from the 48 V available on the transmission twisted pair.

BACKGROUND

Data has been transported over telephone lines for years, but the techniques for compressing the data into the voice bandwidth are getting more elaborate and expensive as data rates increase. Digital telephones simplify the task by directly sending high-speed digital data over the wires for distances of up to 2 km. The data is combined with voice information digitized by the codec/filter and signalling. This combined signal is transported over existing wiring to a digital linecard in a PBX or a voice/data multiplexer.

Digital PBXs used with analog telephones convert analog voice information into digital signals on the linecards for routing through the switch matrix. In a system where the analog telephones are replaced by digital phones, the digitization is still performed, but it is done in the phone itself and digital information is transported on the wires. Data from an attached PC or terminal can easily be combined with the digital voice and be transported to the PBX. At the linecard, the data can either be routed through the switch matrix or separated from the voice and connected directly to a data-only PBX or computer. Signalling between a digital telephone and the PBX is typically done by packet messages, with a microprocessor in the telephone to interpret the messages. This digital telephone uses traditional tone signalling on the voice channel. Hookswitch status is sent to the PBX on the inbound (to the PBX) link of the 8 kbps Signalling Channel One, and ringing information is sent to the phone on the outbound (from the PBX) link of Signalling Channel One.

This digital telephone could be used with a special digital linecard in a PBX or a voice/data multiplexer. To maintain generality, this application note will describe a system where a multiplexer is used rather than a linecard in a specific PBX system. The general principles, however, can be used in a linecard design. This telephone design has been used with both a digital linecard and a voice/data multiplexer.

The voice/data multiplexer in Figure 1 is described in detail in application note AN949. However, a brief description will be made here. From the PBX's point of view, the multiplexer appears to be an ordinary telephone. The telephone hookswitch is replaced by a relay which is controlled by a signal from the digital telephone. The ringing signal from the PBX is detected, sampled, and transported to the digital telephone where it is amplified and applied to a speaker. Analog voice signals are digitized and reconstructed and applied to the wires connected to the PBX through the duplexer in the codec/filter. Asynchronous data from the computer or data switch is synchronized to the UDLT timing by the DSI and added to the digital data stream. The combined signal is transported to the digital telephone which separates the signals and attaches to the data terminal. DC power is applied to the twisted pair wire at the multiplexer and transported over the wires so no extra power cords are required for the telephone.

The following sections describe the details of the digital telephone. Figure 2 shows a block diagram of the digital telephone set. Figures 3 and 4 are complete schematics of the telephone circuitry and the power supply respectively.

UDLT

The heart of the digital telephone set is the UDLT slave (MC145426). This chip is essentially a modem transceiver which operates over standard twisted pair telephone wiring. A 256 kbps data rate using modified differential phase shift keying (MDPSK) in a half-duplex time compression multiplex or "ping-pong" scheme provides full-duplex 80 kbps transmission. Transmission begins with the UDLT master (MC145422), which is located at the other end of the twisted pair in the voice/data multiplexer, bursting 10 bits of information to the slave. A similar burst is returned from the slave to the master a short time after the master's burst has been demodulated. This exchange occurs 8000 times per second

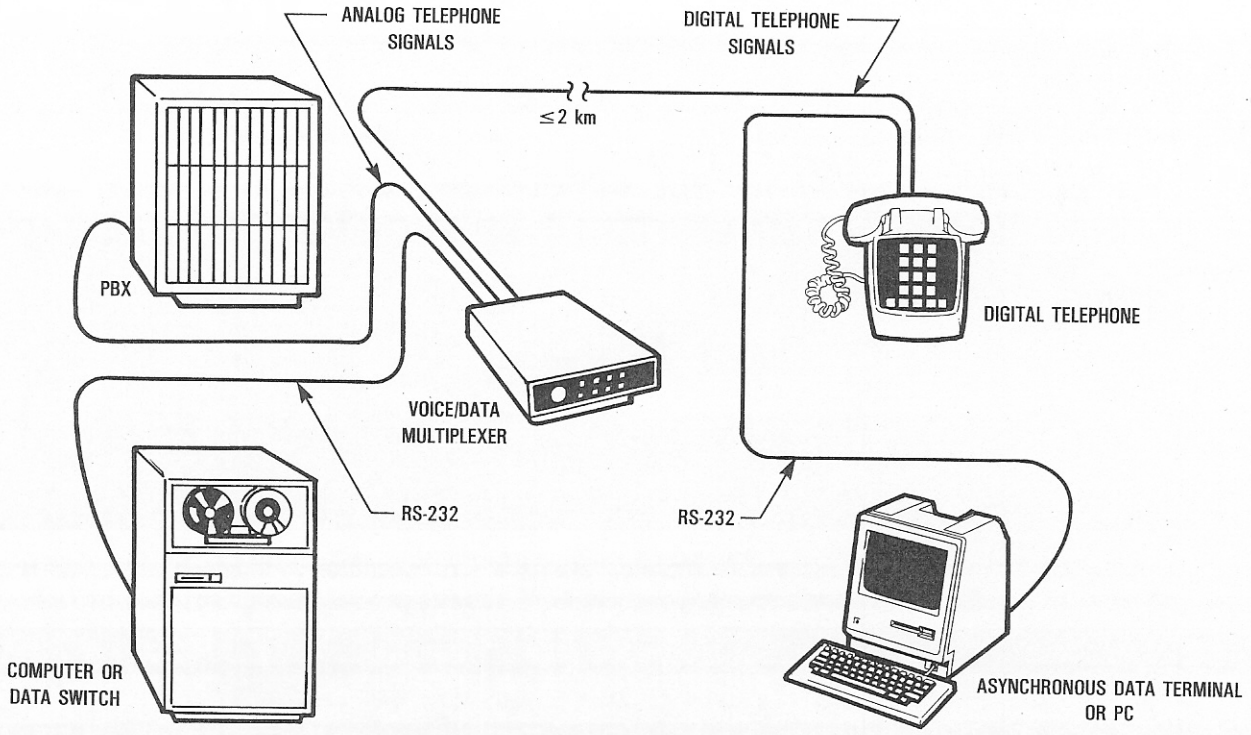


Figure 1. Voice/Data System

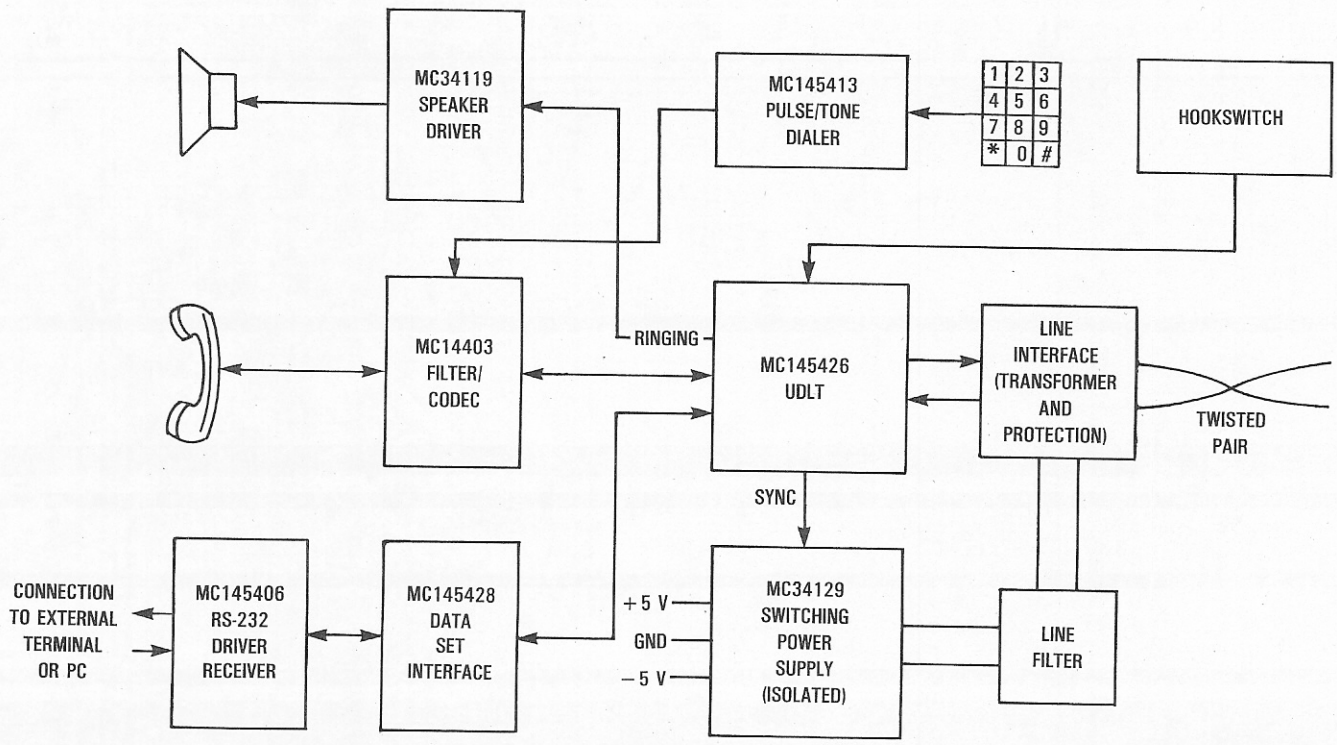


Figure 2. Digital Telephone Block Diagram

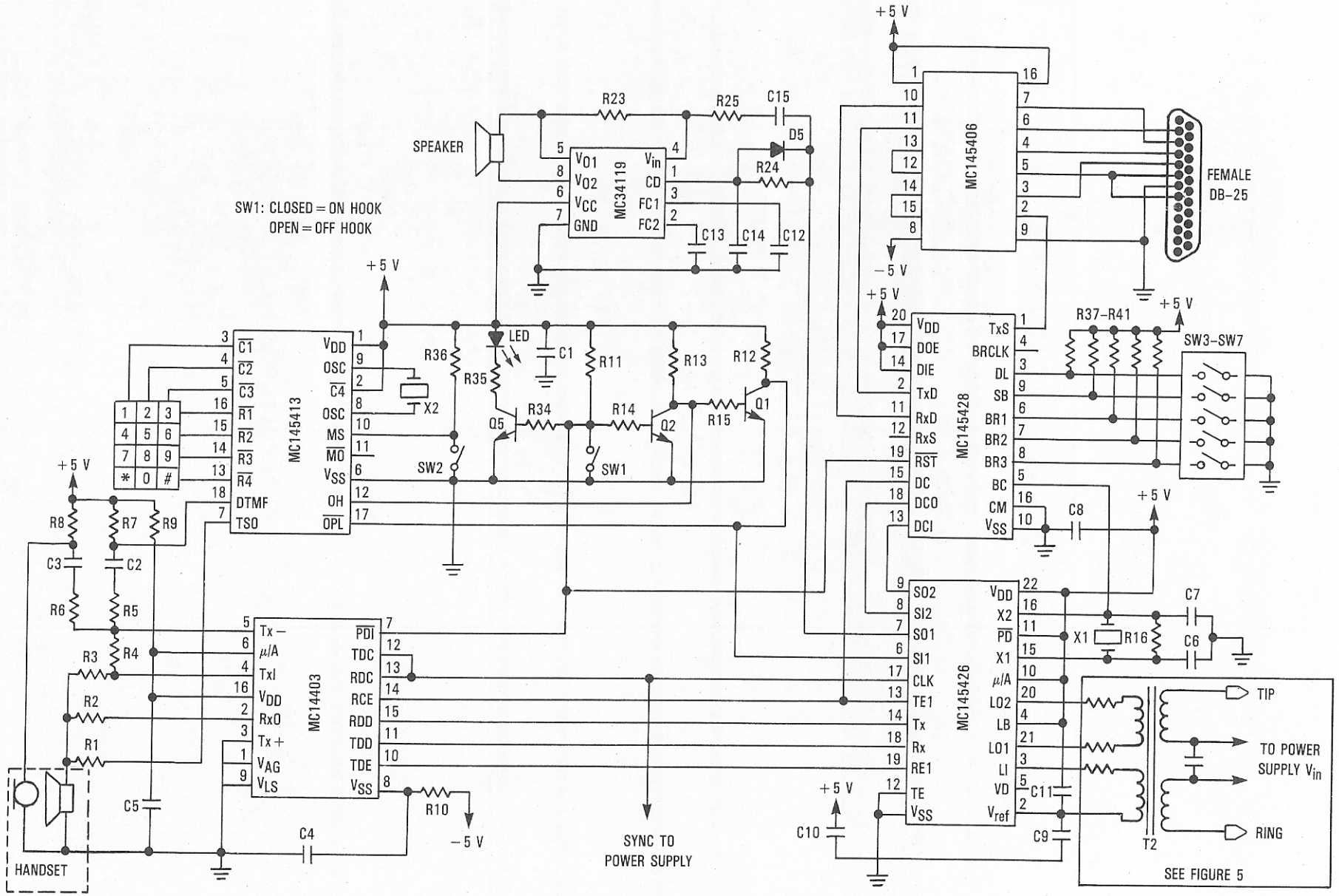


Figure 3. Digital Telephone Schematic

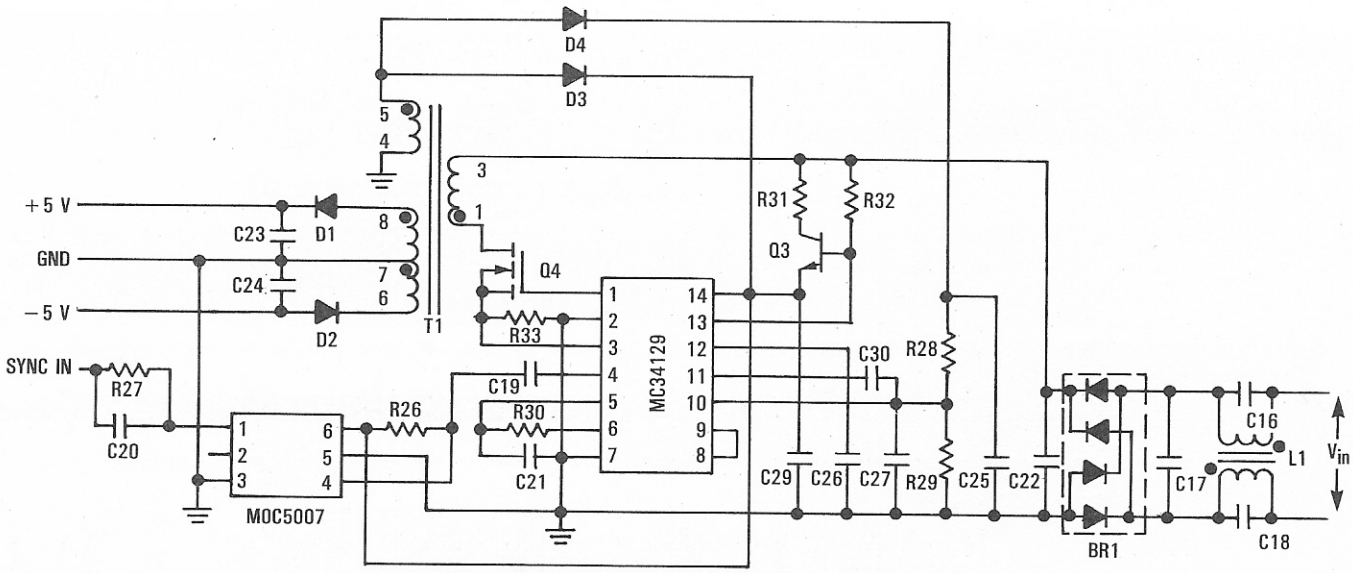


Figure 4. Switching Power Supply

PARTS LIST FOR FIGURES 3, 4, AND 5

Resistors

R1	22 kΩ
R2	3.3 kΩ
R3	7.5 kΩ
R4	47 kΩ
R5	22 kΩ
R6	10 kΩ
R7	620 Ω
R8	1 kΩ
R9–R10	10 Ω
R11–R13	10 kΩ
R14–R15	100 kΩ
R16	10 MΩ
R17	10 kΩ
R18	5 kΩ
R19–R22	110 Ω
R23	75 kΩ
R24–R25	100 kΩ
R26	10 kΩ
R27	3 kΩ
R28	9.1 kΩ
R29	1.3 kΩ
R30	22 kΩ
R31	2.2 kΩ
R32	220 kΩ
R33	10 Ω
R34	100 kΩ
R35	560 Ω
R36–R41	10 kΩ

Inductor

L1 80 μH each winding on a common core

Capacitors

C1–C3	0.1 μF
C4–C5	10 μF
C6–C7	20 pF
C8–C9	0.1 μF
C10	10 μF
C11–C15	0.1 μF
C16	0.005 μF
C17	0.1 μF
C18	0.005 μF
C19	100 pF
C20	0.01 μF
C21	330 pF
C22	100 μF (50 V)
C23–C24	100 μF (16 V)
C25	10 μF (16 V)
C26	0.1 μF
C27	510 pF
C28	0.1 μF
C29	10 μF (16 V)
C30	0.01 μF

Transformers

T1: Power Transformer
Coilcraft G6808-A
T2: Line Transformer
Coilcraft G6320-D or
Lepco P-1358-A

Diodes

D1	1N5819
D2–D11	1N4148
BR1	3N248 Bridge Rectifier

Integrated Circuits

MC14513	Dialer
MC14403	Mono-circuit
MC145428	Data Set Interface
MC145426	Slave UDLT
MC145406	RS-232 Transceiver
MC34119	Speaker Driver
MC34129	Power Supply Controller

Optocoupler

MOC5007 High-speed Optocoupler

Transistors

Q1–Q2	2N3904
Q3	2N5551 160 V NPN
Q4	MTP2N20 Power MOSFET
Q5	2N3904

Switches

SW1	SPST Hookswitch
SW2–SW7	DIP Switches

(every 125 μs), so the transceivers effectively exchange 80 kbps of full-duplex synchronous data. The data is arranged into three channels, a 64 kbps full-duplex voice channel and two 8 kbps full-duplex data channels.

The slave UDLT generates all timing signals used by the digital telephone. Timing is synchronized to the received bursts from the master UDLT. A 4.096 MHz on-chip crystal oscillator is the basis for all clocks. A 128 kHz clock (CLK), which drives the mono-circuit's D/A and A/D circuits and synchronizes the power supply, is produced. An 8 kHz clock (TE1 and RE1) is also produced. Any timing slip from master to slave UDLTs is corrected every 125 μs, keeping the master and slave devices in perfect synchronism. The baud rate generator in the data set interface is driven by the 4.096 MHz clock on the slave UDLT.

The burst received from the master's transmission is input on the slave's line input (LI) pin. The burst is demodulated, separated into the three channels, then output on the digital side of the slave every 125 μs. Eight voice bits are output serially from the transmit data output (Tx) on the rising edges of CLK while TE1 is high. One signalling bit is output on signalling output 1 (SO1) on the rising edge of TE1. The outbound signalling channel one provides the ringing signal for the speaker amplifier (MC34119). The other signalling bit is output on signalling output 2 (SO2) to the data set interface (MC145428), also on the rising edge of TE1. This channel, both inbound and outbound, carries the data between the attached terminal and the data switch or computer at the voice/data multiplexer or PBX.

After the slave receives a burst from the master, it transmits a 10-bit burst of its own back to the master. The slave outputs this burst on its line driver outputs (LO1, LO2) which are push-pull drivers configured as a balanced bridge. These outputs directly drive the line transformer through a resistor loading and protection network (see Figure 5). The 10 bits of data which are transmitted to the master are input every 125 μs. Eight bits of voice data are input serially on the receive data input (Rx) on the falling edges of CLK while receive data enable (RE1) is high. A signalling bit which carries the digital telephone's hookswitch status back to the voice/data multiplexer is input on signalling input 1 (SI1) on the rising edge of TE1. Data from the attached terminal or PC is input on signalling input 2 (SI2), also on the rising edge of TE1.

Transformer T2 interfaces the twisted pair wire to the UDLT's LO1, LO2, and LI pins. It performs the functions of impedance matching, bandwidth limiting, and gain adjustment

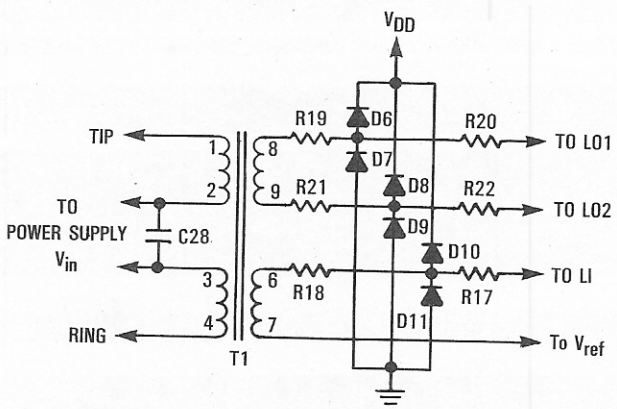


Figure 5. Line Interface and Protection

for the receive signals. At the frequencies of interest (128 kHz and 256 kHz), ordinary telephone wire has a characteristic impedance of about 110 ohms. The loading resistors R19–R22 between LO1, LO2 and the Tx winding of the transformer are set to 110 ohms. The series combination of these resistors is significantly higher than the 20-ohm output impedance of the LO1 and LO2 drivers causing the resistance presented to the transformer to be set primarily by the resistors alone. Clamp diodes D6–D9 protect the LO1 and LO2 outputs from transient signals on the twisted pair. Line settling between data bursts is improved by selecting a bandwidth of 20 to 512 kHz for the transformer interface. The lower corner frequency is set by adjusting the inductance of the transformer's Tx winding to 1.75 mH. The upper corner frequency is determined by the design of the transformer winding technique.

The impedance matching network on the transmit side of the transformer attenuates the transmitted signal by 12 dB. This loss is recovered in the receive side of the transformer. A step-up of 4:1 directly compensates for the 12 dB loss. As with the transmit side, a protection network is required. D10 and D11 clamp the received signal to a safe level but are sufficiently isolated by R17 so that they do not load the transformer when they are conducting. At 192 kHz (the spectral peak of MDPSK), 26 AWG wire attenuates signals about 17 dB/km. The receiver in the UDLTs has sufficient input dynamic range to operate on loops as long as 2 km. Transformers which are designed for the UDLT system may be obtained from:

Coilcraft, Inc.
1102 Silver Lake Rd.
Cary, Illinois 60013
Part Number: G6320-D

Leonard Electric Products Company
85 Industrial Drive
Brownsville, Texas 78521
Part Number: P-1358-A

The transformer from Coilcraft is similar to the Leonard Electric device, except it has a Faraday shield between the Rx and Tx windings and the line windings. The shield helps reduce the spurious radiation from the digital circuitry onto the twisted pair.

CODEC/FILTER

The MC14403 codec/filter is a PCM codec-filter which performs D/A, A/D, band-limiting, and reconstruction filtering for the voice signals in the digital telephone. Analog voice signals in the 300 Hz to 3400 Hz frequency band are sampled at an 8 kHz rate. The samples are converted into a pseudo-logarithmic code known as PCM and passed to the UDLT for transmission to the voice/data multiplexer or PBX. Received digital signals are reconstructed at an 8 kHz rate back into analog voice signals.

Three signals are available for use on the analog input amplifier. They are Tx+ (noninverting input), Tx− (inverting input), and TxI (filter input). Sidetone (feedback from the handset microphone to earpiece) and gain balance are controlled with external components around the Tx and Rx operational amplifiers in the codec/filter. Tx+ is tied to ground and a gain setting resistor is placed between Tx− and TxI.

The microphone output from the handset and the DTMF output from the dialer are both ac coupled to the Tx− input. The output of this amplifier is digitized and output to the UDLT on TDD on the eight rising edges of TDC when TDE is high. Digital data is input from the UDLT on RDD on the first eight falling edges of RDC after the rising edge of RCE. This data is reconstructed and output on the analog output pin (RxO). This signal is summed with TSO from the dialer and TxI and applied to the speaker in the handset.

A decoupling RC filter is used to attenuate any power supply noise seen at V_{CC} and V_{SS} of the codec/filter. This filter consists of 10-ohm resistors in series with the power feed to V_{CC} and V_{SS} with 10 μF capacitors from V_{CC} and V_{SS} to ground. Also, to reduce noise in the ground paths, a star-grounding scheme is used where all ground pins of the circuits are connected to the power supply's central isolated ground.

DATA SET INTERFACE

The MC145428 data set interface (DSI) is an interface between an asynchronous data terminal and the synchronous 8 kbps full-duplex data channel of the UDLT. The DSI performs basic UART functions of start-bit and stop-bit detection of the asynchronous data. It also detects and transports break signals over the synchronous link. Start and stop bits are stripped from the data which is then loaded into a FIFO. The data is then sent to the UDLT for transmission to the far end of the digital link. On the receive side, the reverse of these actions is performed. Special synchronization characters (transparent to the user) are exchanged between DSIs to maintain synchronization. The DSI has an internal clock generator which produces the most commonly used baud rates. The DSI is capable of operating at data rates up to 128 kbps, however this application uses 9600 baud.

On the synchronous side of the DSI, data is output to the UDLT on the data channel output (DCO) on the falling edge of data clock (DC) while the data output enable (DOE) is high. Data from the DSI is input and output by the UDLT on SI2 and SO2 respectively. DC is connected to TE1 of the UDLT. DIE and DOE are connected to V_{DD}, permanently enabling the synchronous inputs and outputs. RESET is connected to the hookswitch, clearing the FIFOs and resetting the device when the digital telephone is not in use.

RS-232 DRIVER/RECEIVER

The RS-232 interface is connected as follows. Asynchronous serial data from the attached data terminal (Tx DATA, RS-232 pin 2) is through a receiver on the MC145406 RS-232 driver/receiver and connected to the transmit data input (TxD) of the DSI. Asynchronous serial data from the DSI is output on the receive data output (RxD) and fed through a driver on the MC145406 to the data terminal (Rx DATA, RS-232 pin 3). Another output of the DSI, transmit data status (TxS), is used to generate a clear-to-send signal for local flow control (CLEAR-TO-SEND, RS-232 pin 5). TxS goes low when there are two words in the DSI's transmit FIFO and must be inverted to provide the CTS function. TxS is applied to a receiver of the MC145406 for inversion and then fed through a driver to convert the signal to RS-232 levels. The MC145406 threshold for the RS-232 receivers is 1.8 volt so it may be used as an inverter for ordinary digital signals. The receive data status (RxS) pin of the DSI may be used as a carrier detector. Since it goes high when synchronization with the far-end DSI is established, it must also be inverted before conversion to RS-232 levels. As with the TxS signal, an RS-232 receiver is used an an inverter. The inverted signal is then converted to RS-232 levels by a transmitter and applied to RECEIVED LINE SIGNAL DETECT, RS-232 pin 8. The baud rate, word length, and number of stop bits used on the asynchronous side of the DSI are controlled by five pins: BR1–BR3, DL, SB. These inputs are controlled by a DIP switch. Table 1 shows the switch settings to configure the asynchronous data port.

DIALER

The pulse tone repertory dialer (MC145413) converts keyboard inputs to either pulses or dual tone multiple frequency (DTMF) or Touch-Tone outputs for use in telephone dialing. This device also provides last number redial and a nine number repertory memory. The digital telephone in this application uses a 3×4 class A single contact keyboard, although a 4×4 keyboard could have been used for enhanced features. The MC145413 operates in pulse mode at either 10 or 20 pulses per second, or tone dialing modes. These modes are determined by the mode select (MS) pin.

When the pulse dialing mode is used in this telephone, dialing information is output at 20 pulses per second. Note: The PBX used with this telephone is capable of accepting dialing pulses at this rate. Other applications may require the pulses at 10 pulses per second, in which case the wiring of the DIP switch would have to be modified appropriately. The pulse output OPL, is an N-channel open-drain transistor which is wire-ORed with the hookswitch. This point is sampled 8000 times each second by the UDLT, and the status is passed to the loop monitoring circuitry in the voice/data multiplexer on signalling channel 1. In the tone dialing mode, dialing information is output as tones corresponding to the row and column pressed. This signal is output on the DTMF OUT pin of the dialer and is coupled to the analog input of the codec/filter. The analog DTMF signal is thus carried to the PBX in digital form on the 64 kbps voice channel.

Table 1. DIP Switch Settings

Pin Name	Low	High
DL	8 bits	9 bits
SB	One	Two
MS	Tone	Pulse

Baud	BR3	BR2	BR1
9600	0	1	1
4800	1	0	0
2400	1	0	1
1200	1	1	0
300	1	1	1

SWITCHING POWER SUPPLY

Figure 4 shows the schematic of the switching power supply for the digital telephone. This power supply has the capability of supplying about 900 mW of power at ± 5 V when the length of the loop is 2 km. As the loop length is increased, the power available at the phone is reduced. To maintain stability of the power supply, the maximum power consumed by the phone (including the efficiency losses in the power supply) must be

less than 90% of the maximum power available (MPA) at the maximum loop length.

$$MPA = V_{source}^2/(4 \cdot R_{loop})$$

Example: R_{loop} for 2 km of 26 AWG wire = 576 Ω

$$MPA = 48^2/(4 \cdot 576\ \Omega) = 1\ Watt$$

The ±5 V outputs are isolated from the twisted pair so that a local ground reference may be established with the terminal attached to the RS-232 port.

The switching power supply operates by repetitively storing and releasing energy in a transformer. The energy is stored in the primary winding of transformer T1 for part of the switching cycle and discharged into the load through the secondary during the remaining part of the cycle. The controller for this power supply is the MC34129 high-performance current-mode power-supply controller. The MC34129 controls the current (energy) in the primary winding by varying the duty cycle of the power switch (Q4). As the duty cycle is changed, more or less energy is stored under control of the MC34129 to maintain regulation of the output voltage. The switching frequency of the power supply is synchronized to the 128 kHz clock signal used by the codec/filter by bringing CLK from the UDLT through an opto-isolator (MOC5007) into the sync input (pin 4) of the MC34129. Synchronization improves the idle-channel noise performance of the codec/filter and minimizes the filter requirements on the output of the power supply.

The input voltage for the power supply is taken from the 48 V available on the twisted pair. A 0.1 μf capacitor is placed between the two line windings of transformer T2. The dc voltage across the capacitor is then routed through a balanced three-pole elliptical lowpass LC filter (L1 and C16–C18) and a full-wave rectifier before being applied to the input of the power supply.

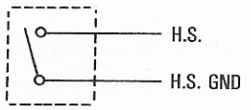
The power supply is regulated by two methods. Current in the primary winding is sensed as a voltage across resistor R30. Also, the +10 V nonisolated output is sensed by being fed back to the voltage divider formed by resistors R25 and R26. The controller maintains the voltage across R26 at 1.25 V by varying the switching duty cycle. This forces the output voltage to be 10 V. Regulation of the +5 V isolated outputs is maintained by the magnetic coupling from the 10 V winding to the +5 V windings. Because the primary current is sensed by the MC34129, pulse-by-pulse overcurrent limiting is automatically achieved. The power supply is thus fully protected against short circuits on the outputs. If an overload occurs, the MC34129 will shut the power supply down and attempt to restart. When the overload is removed, the power supply will again begin normal operation.

During normal operation, the MC34129 is powered by the +10 V output. However, since there is no voltage at this output when the circuit is first started-up, provisions must be made to power the circuit from another source until the outputs are stable. Transistor Q3 and the Start/Run output perform this task. During start-up, Q3 is biased on and power for the MC34129 is taken from the 48 V on the twisted pair through R28. After the power supply has completed the soft-start cycle and stabilized, transistor Q3 is turned off by the Start/Run pin (pin 13) and power is supplied by the +10 V output. This start-up sequence allows the power supply to reliably start in the presence of high source resistance seen at the end of a long twisted pair wire. Efficiency of this power supply is approximately 80%.

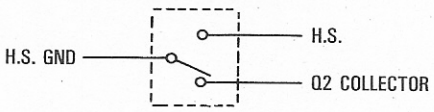
APPENDIX

On the printed circuit board there are three connections available for the hookswitch (SW1). These are +5 V, GND, and SI1. The following is a list of several implementations of the hookswitch.

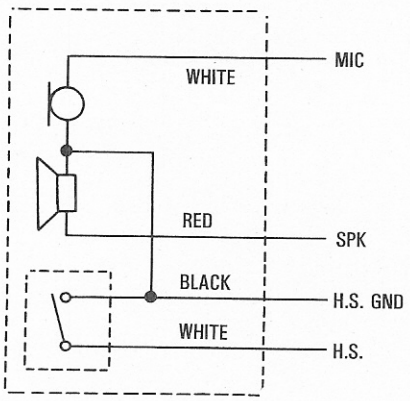
1. **Mechanical SPST switch (normally open)** — In this configuration the LED, R32, R31, and Q5 are not needed unless an LED signal is desired.



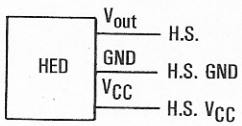
2. **Mechanical SPDT switch (normal position shown)** — In addition to the components listed in the above implementation, R14 and Q2 are not needed.



3. **Reed relay in handset (magnet in telephone case)** — The figure below shows how to modify the handset for this application.



4. **Hall Effect Device in telephone case (magnet in handset)** — For this and the previous application, a mechanical SPST switch can be used in parallel for on-hook operation.



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