AN946

Limited Distance Modem
Using the Universal Digital Loop Transceiver Chip Family

OVERVIEW

The introduction of the Universal Digital Loop Transceiver (UDLT) family of integrated circuits aids the design of a high speed Limited Distance Modem (LDM). With an external clock, the LDM will transmit asynchronous data at rates up to 80 kbps. As shown here with an internal clock, the LDM can send as much as 38.4 kbps of asynchronous full duplex data up to two kilometers on 26 AWG twisted pair wire. The data transfer is controlled by the following RS-232C handshake signals: Request to Send (RTS), Clear to Send (CTS), Data Set Ready (DSR) and Carrier Detect (CD). If the data link is operating, CTS goes active in response to RTS going active. DSR is active if the LDM is powered up. If synchronization is lost, the CD signal goes inactive. Figure 1 shows a block diagram of the LDM. Figure 10 is a photostat of the LDM Demonstration Board - front, and Figure 11 is a photostat of the LDM Demonstration Board - back. Table 1 is a parts list for the slave and master LDM.

UNIVERSAL DIGITAL LOOP TRANSCEIVER

The heart of the LDM is the UDLT master/slave chip set. This chip set transmits data at a 256 kbps burst rate using a "ping pong" approach. As shown in Figure 2, a Modified Differential Phase Shift Keyed (MDPSK) data burst is transmitted from the master to the slave. Then after a slight delay, a burst is transmitted from the slave to the master. Since an eight kHz clock is typically applied to the Master Sync Input (MSI) pin, and ten bits are sent to the master and the slave every MSI period (every 125 μs), the transceiver is effectively transmitting 80 kbps of full duplex synchronous data.

The burst's ten bits of digital data are input on three different pins of the UDLT master. The first eight bits are serially received from the Receive Data Input (Rx) pin. The ninth bit is from the Signaling Bit Input (SI1) and the tenth bit is from the SI2 pin. These ten bits are formatted together and shipped out from the chip on the LO1 and the LO2 pins (Line Driver Outputs). After being transmitted across the line and received on the LI pin of the slave UDLT, eight bits of data are serially output through the slave's Transmit Data Output (Tx) pin, one bit on the SO1 and one bit on the SO2 (Signaling Bit Output). Then the slave UDLT sends a similar burst to the master UDLT.

DLT VS. UDLT

Since the MC145418/19 Digital Loop Transceiver (DLT) chip set is very similar to the UDLT, it is not difficult to adapt

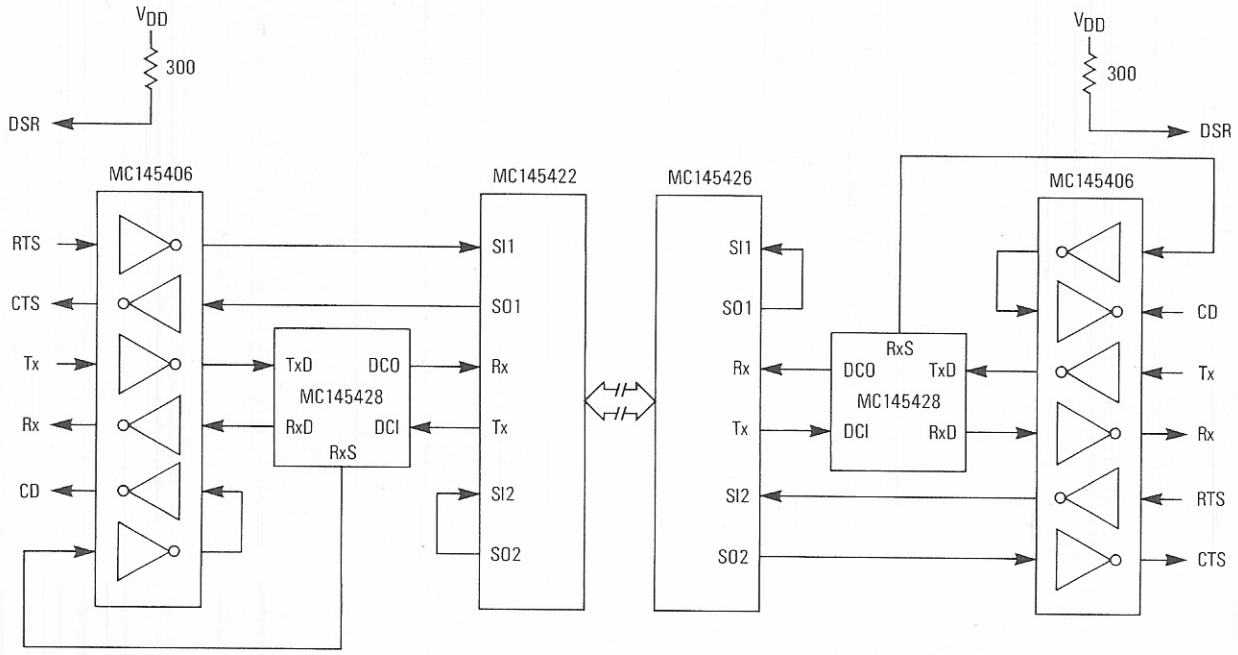

Figure 1. Limited Distance Modem Block Diagram

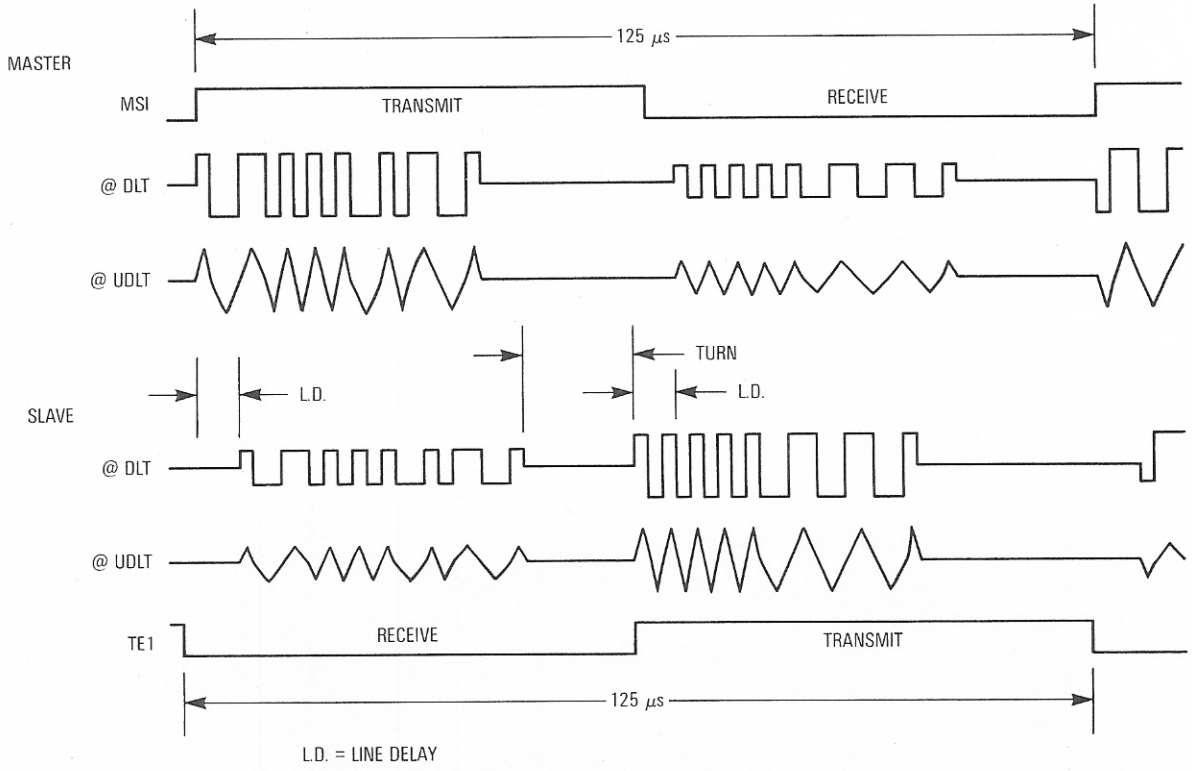

Figure 2. 80 kbps MDPSK Timing Diagram

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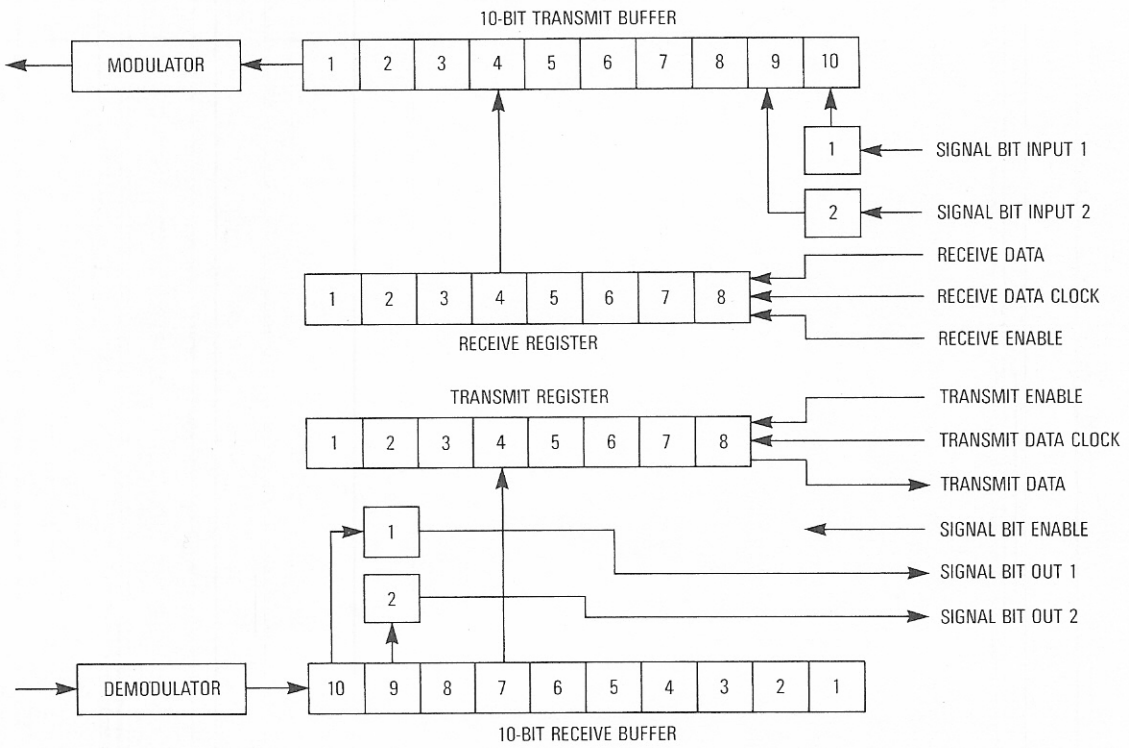

Figure 3. UDLT Receive and Transmit Registers

AA8929-1

this LDM to use the DLT. There are three main differences between the UDLT and the DLT chips. The most important difference between the chips is that the UDLT automatically adjusts the thresholds on the receive circuitry. This allows the UDLT to optimize its reception to a particular line's attenuation level. The DLTs threshold is externally set , so typically this receive optimization will not be achieved, unless some rather complex circuitry is implemented. Also, the DLT requires external drivers and transmits square waves instead of triangular waves. In conclusion, the UDLT has on board driver and threshold adjust circuitry, but the DLTs basic approach allows driver and threshold design flexibility.

SIGNALING PINS FOR RTS/CTS HANDSHAKE

This LDM uses the SI1, SI2, SO1 and SO2 pins of the master and slave for a RTS/CTS handshake. To perform this task, the signaling channels are used for transmitting the RTS/CTS handshake. The input at SI1 of the master UDLT is the RTS signal. This information is transmitted to the SO1 of the slave UDLT chip. At this point, the signal is looped around into SI1 of the slave UDLT, and it is transmitted to SO1 of the master UDLT. This signal at SO1 is the master's CTS signal. A similar configuration is used for the slave's RTS/CTS handshake on the SI2/SO2 channel. This allows the RTS/CTS handshake to verify that the communication link is operating.

DATA SET INTERFACE

Since most data from a terminal is an asynchronous format, the Data Set Interface (DSI) is needed to convert data from an asynchronous to a synchronous format and vice versa. At TxD of the DSI, the asynchronous signal should begin with a start bit (logic 0). After following with an eight or nine bit data word, the format ends with one or more stop bits (logic 1). The rate that the data is loaded into the DSI is determined by the internal bit rate generator, whose rate, if 38.4 kbps or less, is selected by BR1, BR2 and BR3 (Baud Rate Select Pins). An external bit rate generator can be used for data rates higher than 38.4 kbps.

Once in the DSI, the data is stripped of its start and stop bits and loaded in a register. Next, the data is checked for a break condition, and one of three types of words is sent, under the timing control of the DC, CM and DOE pins. If a break condition is recognized, the break flag (11111110) is transmitted. If data is in the register, it is dispatched. Finally, if no data is in the register, a synchronizing flag (01111110) is sent. However, regardless of data being in the transmit register, a synchronizing flag is also transmitted on a regular basis to verify that synchronization is intact. Furthermore, the transmit circuitry inserts a binary 0 after five continuous 1's of data, so neither pattern, (11111110) or (01111110), can be sent as data.

At DCI, DC, CM and DIE control the synchronous data's receive loading into the DSI. Once loaded, the DSI's receiver determines if the data is break or synchronizing information. If it is a break or synchronizing flag, the appropriate action is taken. If it is not, the data is loaded into a receive register. From this register, data words are taken, start and stop bits are added and the asynchronous word is output on RxD (Receive Data) at the baud rate selected by BR1, BR2 and BR3. Figure 4 is a block diagram of the DSI.

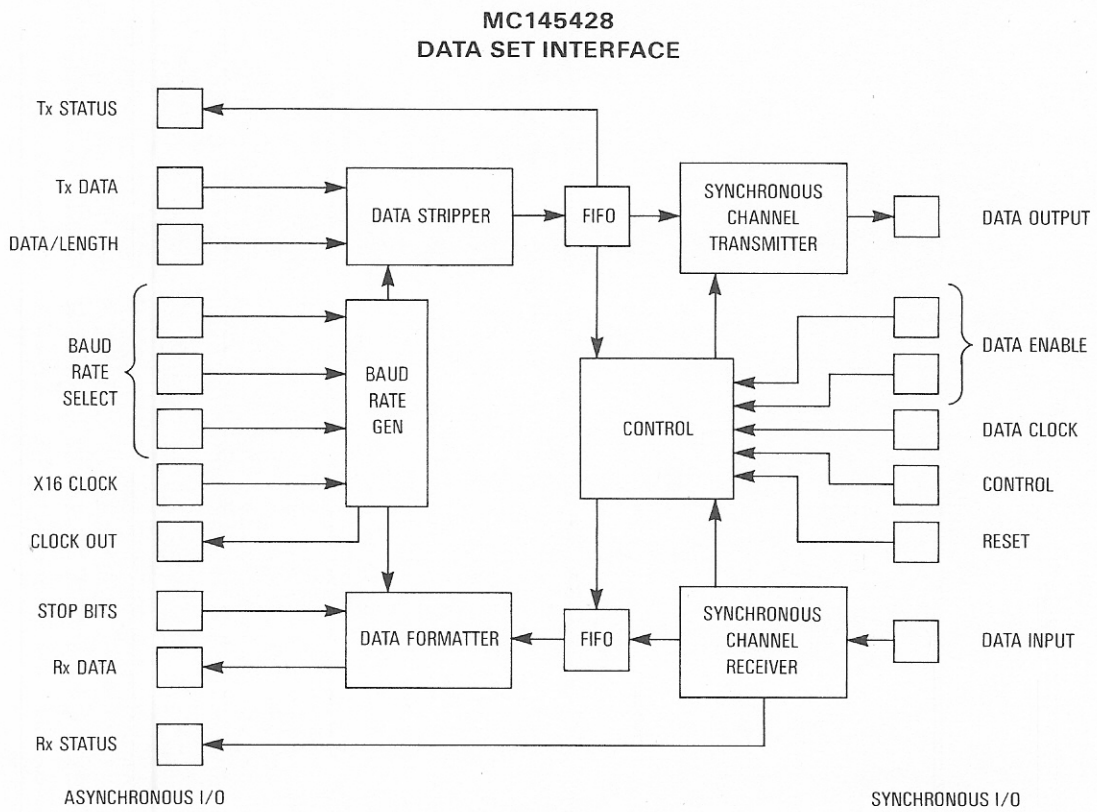

Figure 4. DSI Block Diagram

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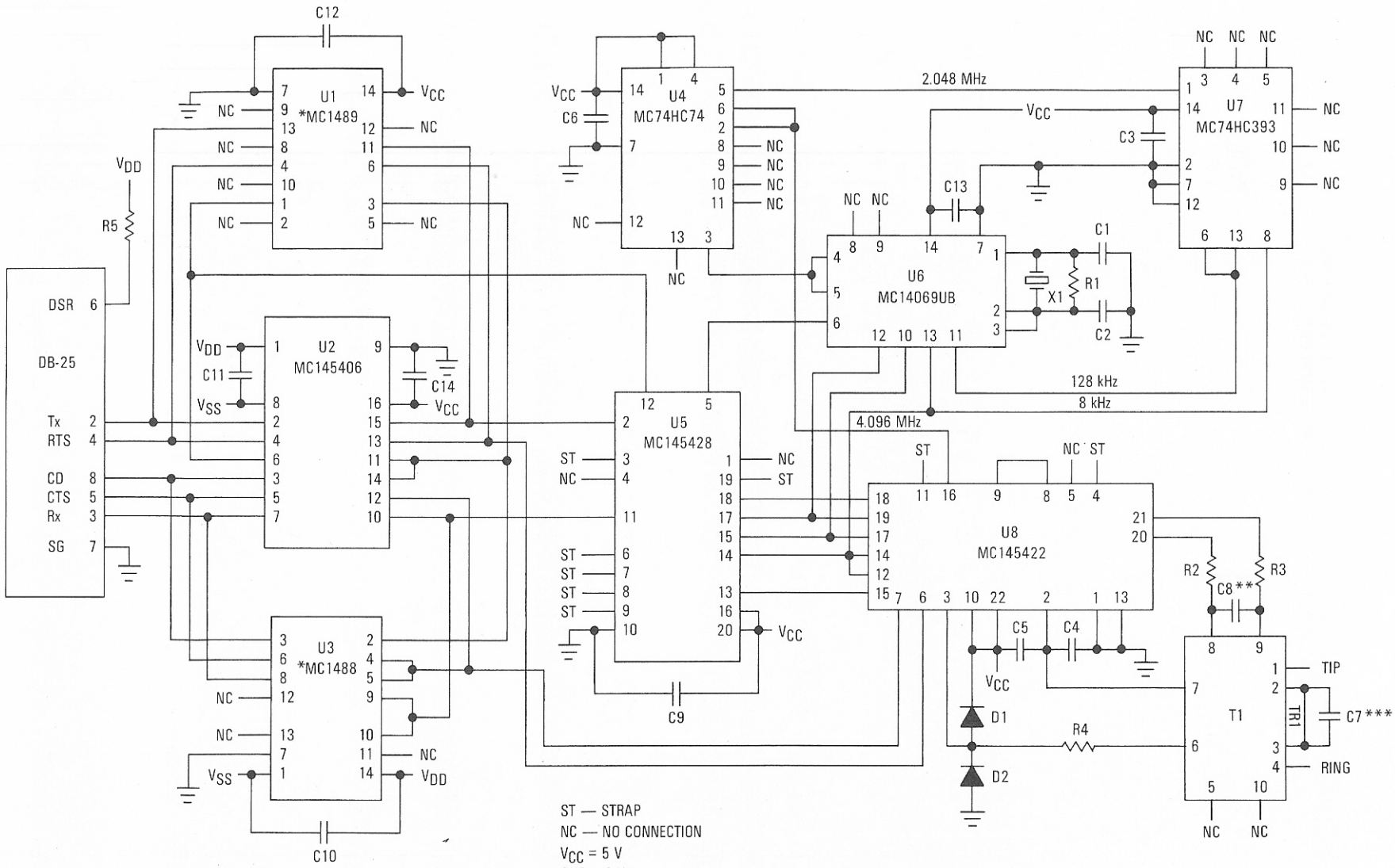
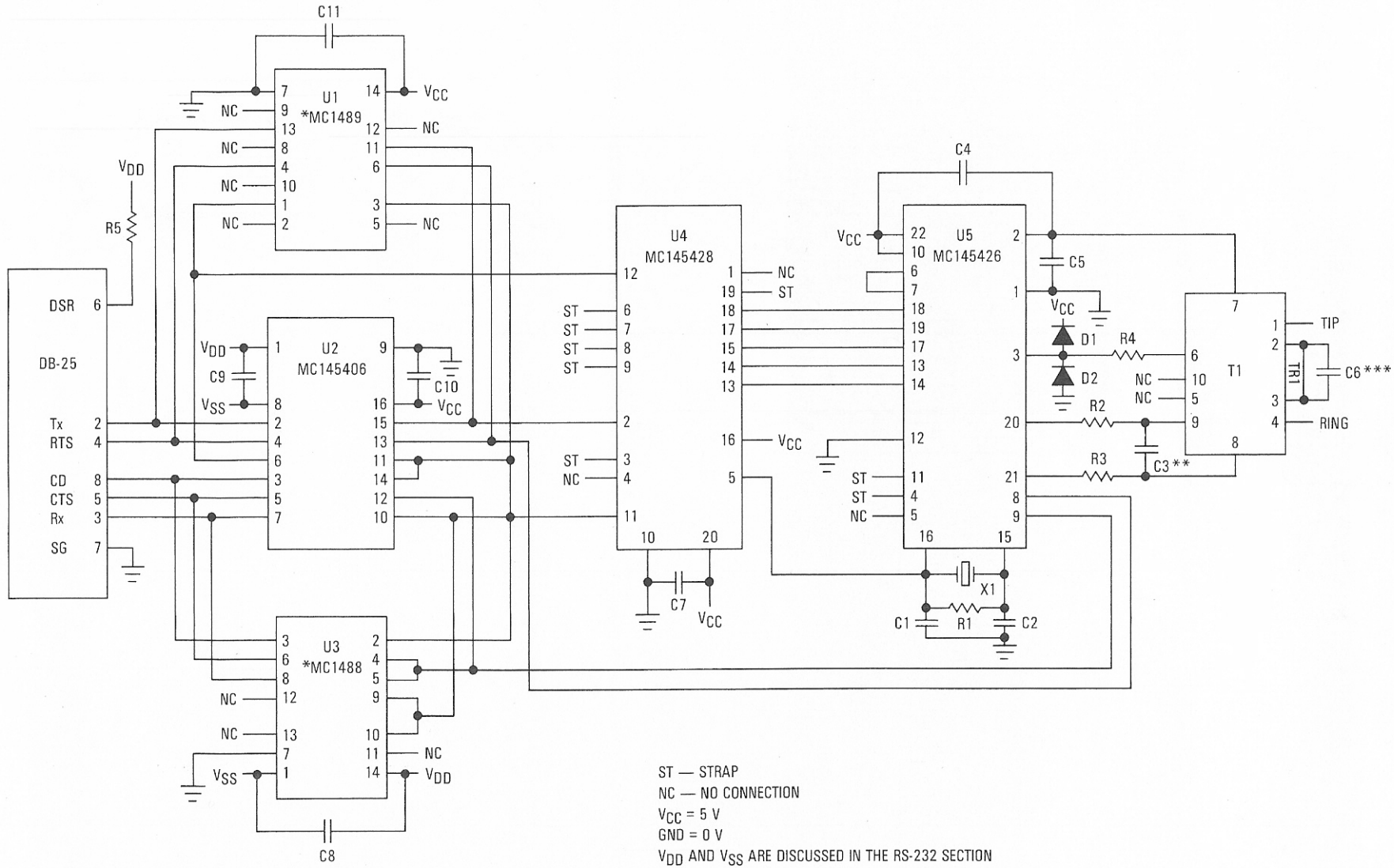


ST — STRAP
NC — NO CONNECTION
V_{CC} = 5 V
GND = 0 V
V_{DD} AND V_{SS} ARE DISCUSSED IN THE RS-232 SECTION

*MC1489 and MC1488 used when MC145406 not used
**C8 is optional filtering.
***TR1 should be cut when C7 is used

Figure 5. Master Limited Distance Modem



*MC1489 and MC1488 used when MC145406 not used

**C3 is optional filtering.

***TR1 should be cut when C6 is used

Figure 6. Slave Limited Distance Modem

RS-232C DRIVER/RECEIVER

The last integrated circuit discussed is the RS-232C interface. Either the MC145406 or the MC1488/MC1489 Driver/Receiver, which both fulfill the electrical specifications of EIA Standard RS-232C and CCITT Recommendation V.28, can be used. The receivers invert the signal and convert the RS-232 signals to standard five volt logic levels, and the drivers invert the signal and convert five volt logic levels to RS-232 voltage levels.

The MC145406 is a CMOS RS-232 chip with three drivers and three receivers. This chip operates with a five volt supply and ±5 to ±12 volt supplies. Although the MC145406 chip will work with ±5 volt supplies in most systems, the voltage supplies should be at least ±7 volts to meet the RS-232 driver specification. For full RS-232 compliance, the driver's output must be between 5 volts and 15 volts for a logical 0, and it must be between –5 volts to –15 volts for a logical 1.

The MC1488 is a quad line driver. For the MC1488 to comply with the RS-232 driver requirements, a minimum power supply of ±8 volts must be used. However, the chip will operate effectively in most systems with the positive supply voltage varying from +7 to +15 volts. The MC1489 is a five volt quad line receiver.

RS-232C CONTROL AND SIGNALS

As seen in Figure 5, the master LDM schematic, and Figure 6, the slave LDM schematic, asynchronous control and data signals enter the LDM at RS-232 voltage levels through a DB-25 connector. Figure 7 shows a DB-25 connector which is the standard computer terminal connector. Pins 2,3,4,5,6,7,8 transmit the following information:

Pin 2: Transmit Data (Tx)
Pin 3: Receive Data (Rx)
Pin 4: Request to Send (RTS)
Pin 5: Clear to Send (CTS)
Pin 6: Data Set Ready (DSR)
Pin 7: Signal Ground (GND)
Pin 8: Carrier Detect (CD)

The Tx and RTS signals are fed into the receivers, and the Rx, CTS and CD signals are outputs of the driver. For the CD signal, one of the receivers inverts the signal from the RxS pin of the DSI. When the DSI is in asynchronous status, this inversion gives the CD a logic 0. The output of that receiver is then put into a driver to obtain RS-232 voltage levels. The DSR pin is connected to the RS-232 positive power supply through a 300 ohm resistor. Therefore, DSR will go active whenever the power supply is on. The GND pin is connected to the system's ground. The remaining pins used of the DB-25 connector are routed to the RS-232 Driver/Receiver.

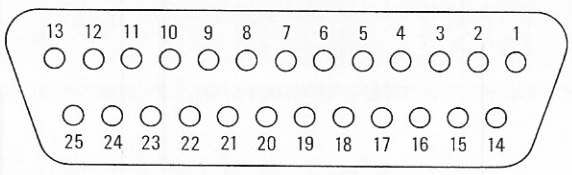


Figure 7. DB-25 Connector

TRANSFORMER INTERFACE

The transformer interface greatly affects the UDLTs capabilities. It performs the functions of impedance matching, bandwidth limiting, increasing receive voltages to required threshold levels and input protection. At 256 kHz, 26 AWG wire's characteristic impedance is 110 ohms. The source resistors from the LO1 and LO2 pins are chosen to be 220 ohms. With a transformer turns ratio of 2:1, the line side's characteristic impedance is 110 ohms. This configuration impedance matches the twisted pair.

The UDLTs minimum output voltage from the LO1 and the LO2 pins is 2.25 volts peak. Half of the voltage is lost across the 220 ohm source resistor. That voltage of 1.12 volt peak is halved again by the 2:1 turns ratio of the transformer to 0.56 volts peak. At 256 kHz, 26 AWG wire attenuates a signal level of 18 decibels-per-kilometer. After traveling a distance of two kilometers the signal will have attenuated 36 decibels. At the line side of the transformer, the minimum signal level is 8.9 millivolts peak. A turns ratio of 1:4 in the transformer windings brings the signal level up to 35.6 millivolt peak. This voltage is divided between a resistor from the transformer to the LI pin and an internal resistance. At worst case, 29 millivolt peak are at the LI pin — within the 25 millivolts peak minimum allowed signal.

The UDLTs maximum voltage output is 3.0 volts peak. Because of the voltage being halved by the source resistors and the transformer windings, the transmit signal level at the line side is 0.75 volt peak. With a short loop, the signal level drop is negligible, so the signal level at the receiving transformer is about 0.75 volts peak. With the 1:4 turns ratio at the receiving transformer, the signal level at LI will be 3.0 volts peak, which exceeds the 2.5 volt peak maximum input at LI. A signal level greater than 2.5 volts peak will inject current into the UDLTs substrate. This action will distort the modulator's output, thus creating bit errors. Consequently, protection diodes and resistors are needed to clamp the input at LI. The demonstration board's transformer configuration is shown in Figure 8. The LI pin's protection includes a 1 kilohm resistor between the LI pin and the diodes. This resistor is not on the

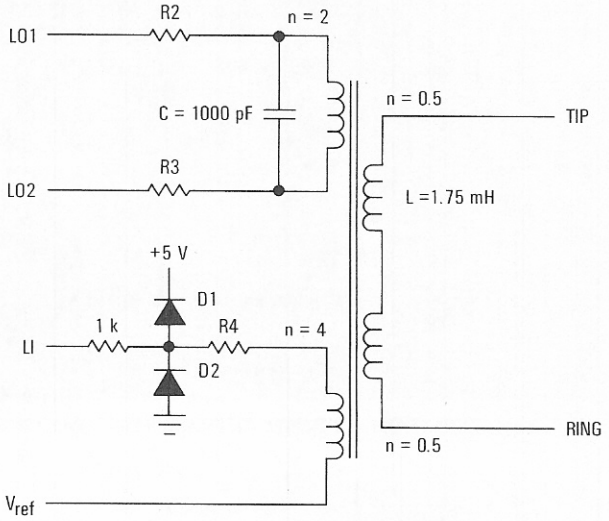


Figure 8. Transformer Configuration Used in LDM Schematic

demonstration board. Typically, the external diodes will turn on before the chip's internal diodes, so the external diodes will shunt most of the current. However, the 1 kilohm resistor will further ensure that the external diodes turn on first.

The maximum power bandwidth of the UDLT is 8 to 512 kHz, but to improve line settling, it is desirable to use a 20 to 512 kHz bandwidth. To make the lower corner of the bandwidth 20 kHz, the inductance of the transformer windings is chosen to be 1.75 millihenries. To make the upper corner of the bandwidth 512 kHz, a 0.001 microfarad capacitor is placed in parallel with the transmit tap. If battery feed is used, further input protection is advised. Figure 9 shows a more durable transformer configuration. Transformers fulfilling these specification can be obtained from:

Leonard Electric Products Company
85 Industrial Drive
Brownsville, Texas 78521

Part Number: P/N P-1358-A

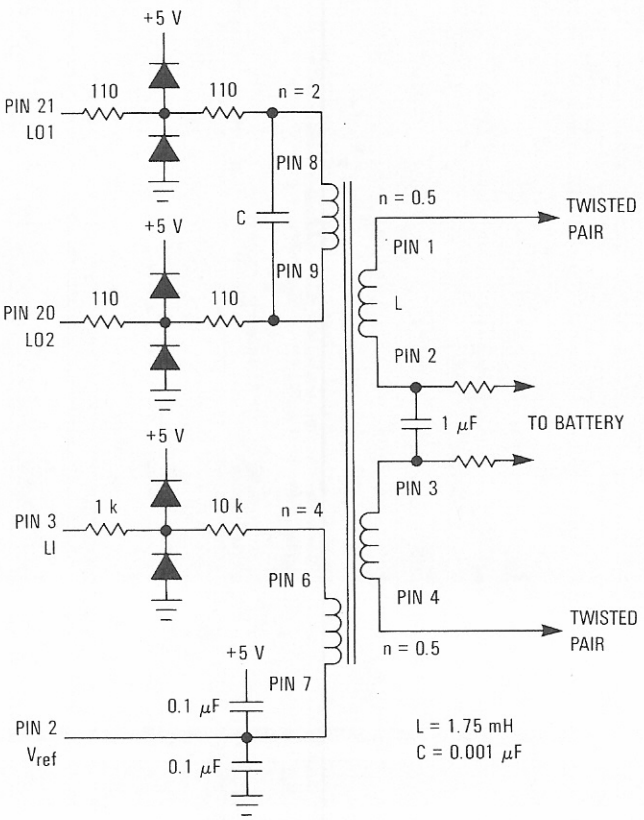


Figure 9. Battery Feed Transformer Configuration

LDM BOARD OPTIONS

A picture of the LDM demonstration board is shown in Figure 10 and 11. Many of the UDLT and DSI features are made available on the demonstration board using straps. These UDLT features include:

$\overline{LB}$: In the master, a low disconnects the LI pin from the internal circuitry, drives LO1, LO2 to V_{ref} and internally ties the modulator to the demodulator. In the slave, a low on the $\overline{LB}$ pin makes the incoming demodulated data going to Tx replace the incoming data on Rx.

$\overline{PD}$: A low powers down the UDLT, except for the receive circuitry.

The DSI features that can be controlled using the straps include:

SB: A low selects outputting one stop bit per data word, and a high selects outputting two stop bits.

DL: A low selects operating with eight bit data words, and a high selects operating with nine bit data words.

Reset: A low clears the internal FIFO, disables TxD, and forces TxS and RxS low.

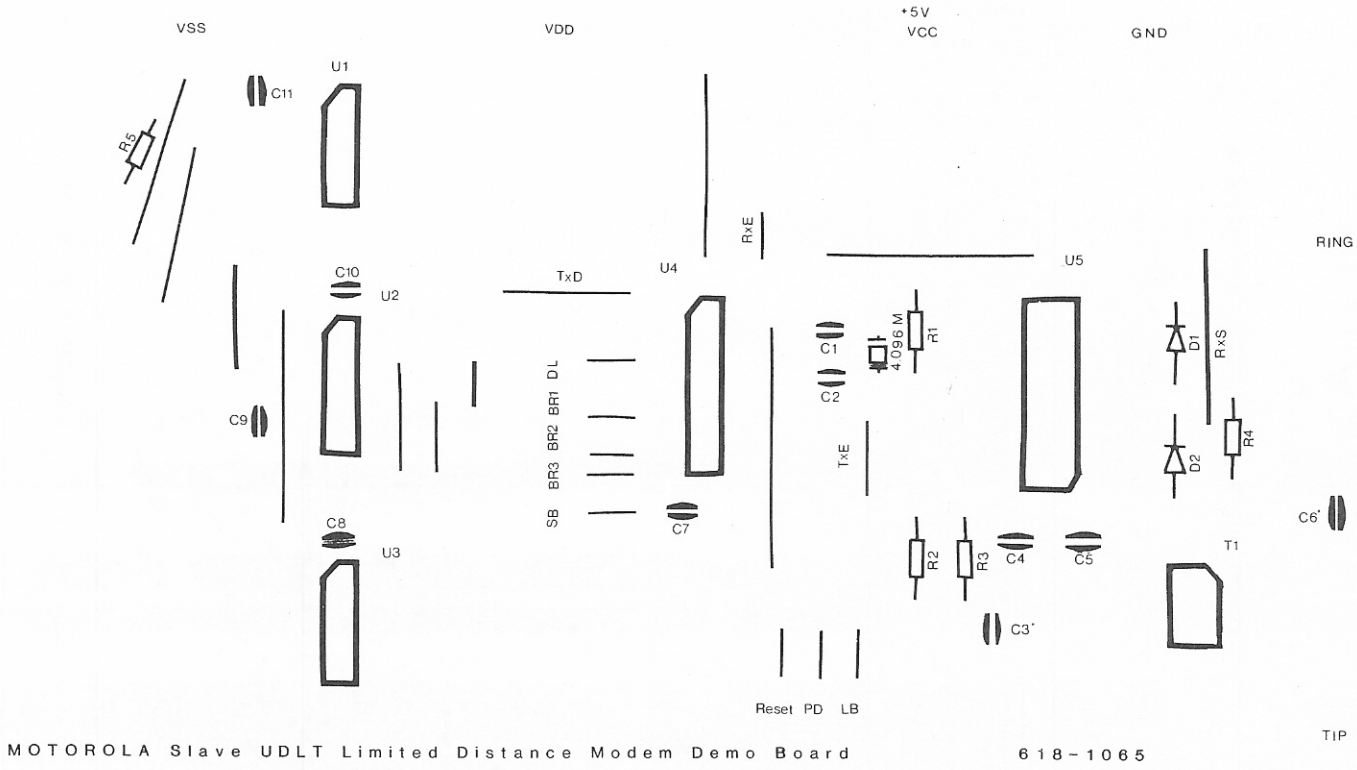
BR1, BR2, BR3: These pins select the asynchronous data rate.

For more information, refer to the individual data sheets. The top of the LDM board shows suggested straps for these functions. These straps select one stop bit, an eight data word, an inactive Reset, a 9600 baud asynchronous data rate, an inactive loop-back and an inactive power-down.

For battery feed applications, C6 of the slave LDM and C7 of the master LDM can be inserted, and the trace between these pins should be broken. This capacitor allows ac signals to pass through the transformer, but keeps dc power across the capacitor to be fed into the system's power supply. C3 of the slave LDM and C8 of master LDM provide filtering for the upper corner of the bandwidth. If this filtering is not desired, these capacitors may be omitted, but their insertion is recommended.

CONNECTORS

On the demonstration board, V_{SS} and V_{DD} are only used to power the RS-232 circuitry. V_{SS} is the most negative power supply, and V_{DD} is the most positive power supply. The RS-232C Driver/Receiver section explains the appropriate voltage ranges for using either the MC145406 or the MC1488/MC1489. V_{CC} is the board's five volt supply, and GND is the board's digital ground. Tip and Ring are the connections for the twisted pair wire. The 25 pins on the left side of both the slave and the master board is for the DB-25 connector.



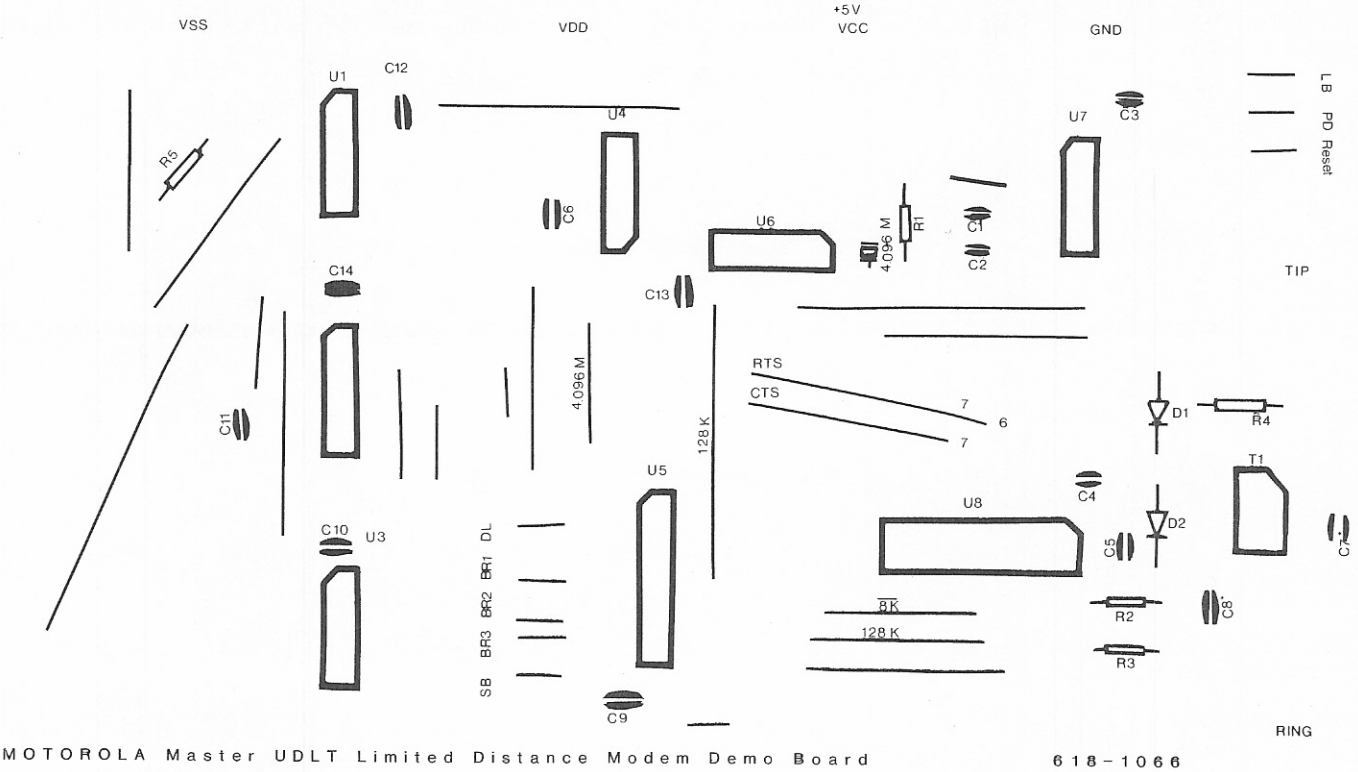
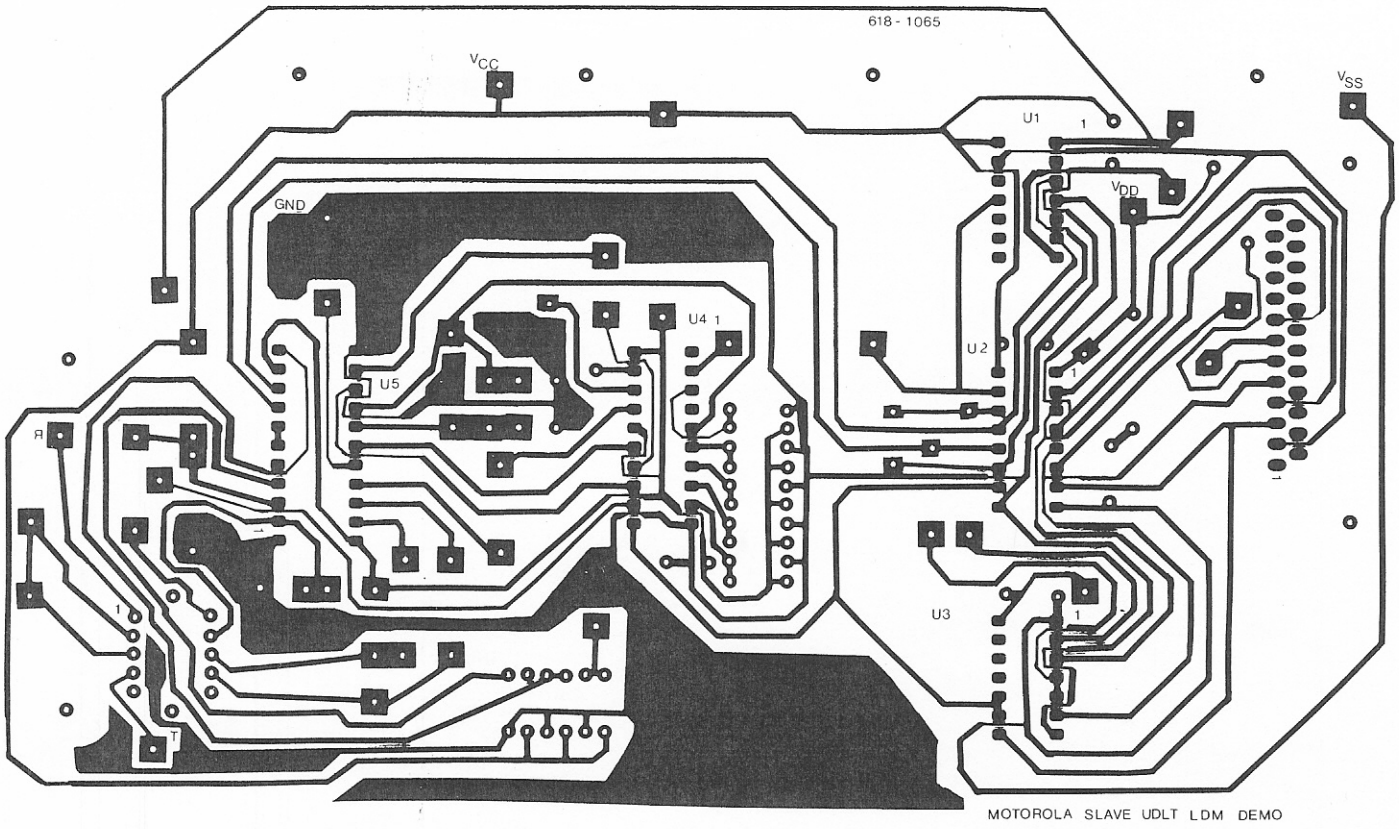
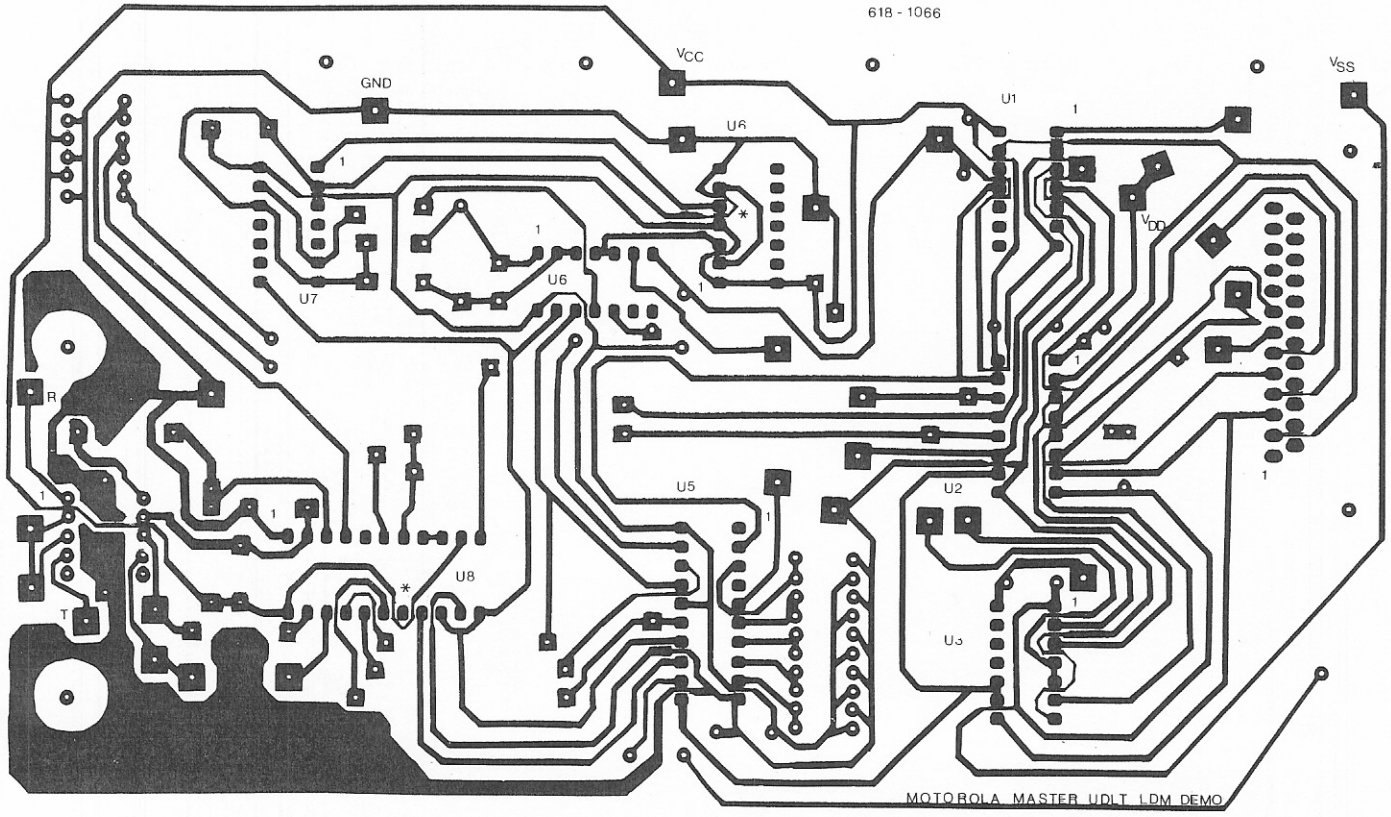


Figure 10. Photostat of LDM Demonstration Board - Front





*External to the demonstration board-back, pin 6 of the MC74HC74 should be connected to pin 16 of the MC145422

Figure 11. Photostat of LDM Demonstration Board - Back