MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN943

UDLT Evaluation Board

INTRODUCTION

To help meet the demands for a cost effective solution to the ever growing voice/data world within the digital telephone and PBX realm, Motorola has created the Universal Digital Loop Transceiver (UDLT) voice/data circuit family. The purpose of this application note is to render an understanding of the UDLT voice/data family and show a typical application for these CMOS parts. This is an evaluation of the application and performance of the MC145422/26 UDLT demonstration board, which was designed and built for customer evaluation.

FUNCTION OF PARTS

UDLT's

The UDLT master (MC145422) and slave (MC145426) are transceivers that provide 80 kilobit-per-second full duplex synchronous voice and data communication to distances of two kilometers on 26 AWG twisted pair and further on heavier gauge pairs. The modulation technique used is a 256 kilobaud Modified Differential Phase Shift Keying (MDPSK) type burst. The MDPSK triangular waveform used in this modulation technique reduces radiation, EMI, and crosstalk due to its compact frequency spectrum.

The master which is used at the telephone switch linecard bursts ten bits to the slave, consisting of eight bits of voice/data and two signaling bits. The slave, which is used at the terminal or digital telephone, receives the burst from the master and upon demodulation of the burst synchronizes its clocks, and bursts ten bits back to the master. This "ping-pong" technique occurs within a 125 microsecond frame period and allows end to end full duplex, synchronous operation. This full duplex operation between the master, at the digital linecard and the slave/mono-circuit, at the digital telephone, enables each set to have high speed access to the PABX switching facility.

At the linecard a microprocessor has complete control of the master. The Signal Enable input (SE) is a three state controller pin which if held high enables the power down, loopback and the two signaling bits, thus allowing these signals to be bussed to the microprocessor. The master can be programmed via the Signal Insert Enable (SIE) pin to insert signaling bit two into the LSB of the PCM word at Tx. This allows simultaneous voice and data transmission through the PABX without the need of changing existing hardware and software. Both the master and the slave have power down and loopback features for system power conservation and testing. The power down pin on the slave is a bidirectional pin. It can be used as an input to initiate a call. When the PD pin is pulled high, the slave will continue to burst every other frame (once every 250 microseconds) until the master responds by bursting. Once the master responds, the slave synchronizes to ping-pong with the master at an eight kilohertz rate. The PD pin can be left floating as an output, in which case the slave will pull PD high until the slave stops receiving bursts from the master then it will take PD low and stop bursting until PD is brought high or the master bursts again. A three state control can be used on this pin if the designer wants to send data to the master during a power down. The slave also has a Tone Enable input pin (TE) which when held high generates a 500 hertz square wave tone at approximately −20 dBm0 which can be used in the digital telset to provide audio feedback.

MONO-CIRCUITS

Motorola's family of Pulse Code Modulation (PCM) mono-circuits incorporate a codec, filter and voltage reference into a single IC. The general block diagram for Motorola's mono-circuits is shown in Figure 1. These devices perform the digitizing and recovery, as well as the band-limiting and reconstruction filtering necessary for voice digitization in telephone systems. The mono-circuits are tailored for a variety of telephone switch architectures. The family consists of five different device types. The MC14400, MC14403, and MC14405 16 pin devices, the MC14401 18 pin device and the MC14402 22 pin device allow designers to optimize for minimal configurations or select a full set of features. The MC14403, for example, can be used where minimal space is desired for the digital phone design whereas the MC14402 is available for maximum flexibility. The mono-circuit incorporates the band-pass filter required for antialiasing and 60 hertz rejection, the A/D, the D/A, both for either U.S. Mu-Law or European A-Law companding formats, the lowpass filter required for reconstruction smoothing, on-board precision voltage reference and does not require any external components.

In this demonstration board, the full featured 22 pin MC14402 mono-circuit is used in the slave circuit showing its ability to adjust the receive gain while maintaining a low impedance output using the RxO, RxG, and $\overline{\text{RxO}}$ pins, The MC14403 is used on the master board showing a simple 16 pin solution for the telephone handset interface.

DATA SET INTERFACE (DSI)

The MC145428 Data Set Interface (DSI) provides the asynchronous to synchronous and synchronous to asynchronous data conversion. This low power five volt CMOS device is ideally suited to interface between the RS-232 compatible data port of any voice/data digital telset or terminal and the synchronous data channel of the UDLT. A block diagram of the Data Set Interface is shown in Figure 2.

There are two basic modes of operation for the synchronous channel interface. In the first mode the DSI inter-

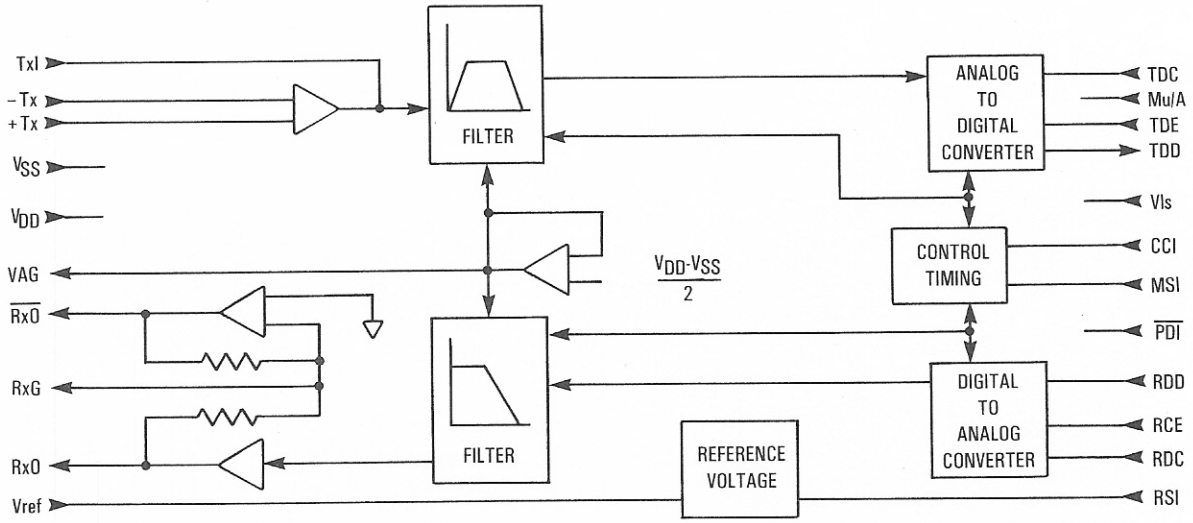


Figure 1. Block Diagram of the Mono-circuits

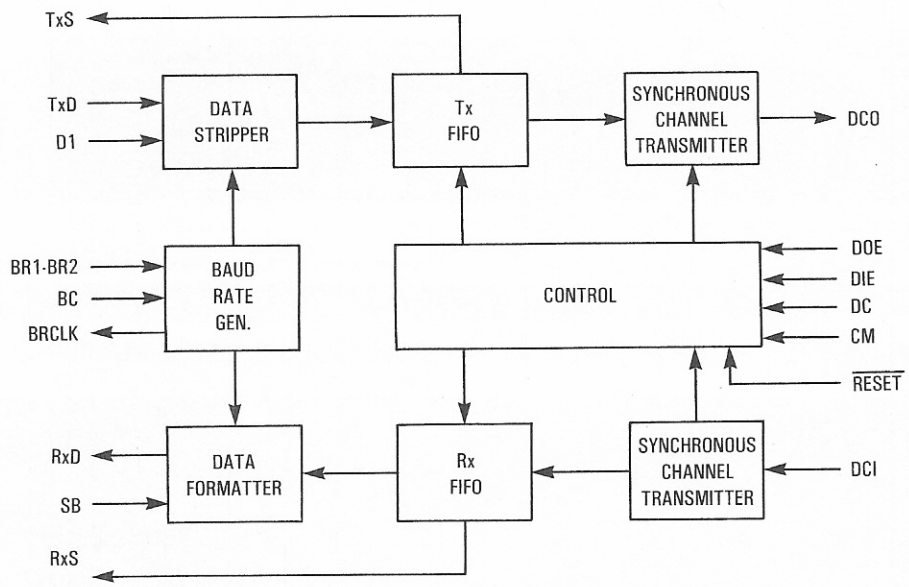


Figure 2. Block Diagram of the Data Set Interface

faces to the eight kilobits-per-second data channel of the UDLT. The Clock Mode input (CM) is tied low while the Data Output Enable (DOE) and Data Input Enable (DIE) are tied high. In this mode a new data bit is clocked out of Data Channel Output (DCO), a new data bit is clocked in at Data Channel Input (DCI), on each falling edge of the Data Clock (DC).

In the second mode of operation, the clock mode is held high. In this mode the DSI is intended to interface with the UDLT's 64 kilobits-per-second data channel. Data is clocked out under control of DOE and the rising edge of DC. Data may be clocked out at a maximum length of eight bits per enable high period. Data is clocked into DCI under control of DIE high and the falling edge of DC. The maximum word size is also eight bits per DIE high period.

Asynchronous data is input on the TxD pin from the output of the RS-232 receiver. This data must have at least one start and one stop bit and at least eight data bits, but will accept nine. The length of the data word is set by the DL pin. A high on DL selects a nine bit data word and a low selects an eight bit data word. The baud rate at which the DSI accepts data on the TxD pin, and outputs data on the RxD pin, is selected with the BR1, BR2, and BR3 pins which derive the internal sampling clock. The internal baud rate generator may be programmed to accept common asynchronous data rates from 300 to 38.4 kilobits-per-second. This internal sampling clock is 16 times the selected baud rate. If BR1-BR3 are all set to logic zero then an externally supplied 16 times clock can be used on the Baud Clock pin (BC) thus giving the user a variable data

rate from zero to 128 kilobits-per-second. For the internal baud rate generator to be accurate, a 4.096 megahertz clock must be used at the BC pin. If the internal baud rate generator dividers are used with a BC clock other than 4.096 megahertz, the data rate may be directly scaled.

Data input on the TxD pin is stripped of its start and stop bits and is loaded into the transmit FIFO register. If the transmit FIFO holds more than two data words or if RESET is held low, then the (TxS) Transmit Status output pin will go low.

Data coming in from the synchronous side is loaded into the receive FIFO, the data has its start and stop bits inserted and is output at RxD at the same baud rate as the transmit side. If the receive FIFO is overwritten, RESET is held low, or if loss of synchronization occurs by the loss of the synchronizing flag word, then the (RxS) Receive Status output pin will transition low.

RS-232 DRIVERS/RECEIVERS

The RS-232 Driver/Receiver chips interface the data terminal equipment with data communications equipment. Motorola manufactures both the MC1488 Quad Line Driver as well as the MC1489 Quad Line Receiver. Both 14 pin packages were used in this evaluation board. Motorola also manufactures the MC145406 Driver/Receiver chip which is a silicon-gate CMOS integrated circuit that combines three drivers and three receivers compatible with the electrical specifications of EIA standard RS-232-C, and CCITT V.28. This part has the capability of running with power supplies ranging from ±5 volts to ±12 volts while operating with a maximum quiescent current supply of 1.45 milliamperes. By combining both the drivers and receivers in a single CMOS chip, the MC145406 provides an efficient, low-power solution for RS-232-C/V.28 applications. A footprint for the MC145406 is included on the evaluation board design.

TRANSFORMER INTERFACE

The transformer interface between the UDLT and the twisted pair wire is of primary importance. The major transformer specifications can be determined from the specifications of the UDLT, driver/receiver, modulation technique, effective characteristic impedance of the wire, attenuation of the wire and dc current feed capacity. The UDLT has a differential output (LO1, LO2) that can drive 440 ohms differentially to five volts peak to peak. The receiver has an input threshold of ±25 millivolts. The UDLT modulation method has maximum power bandwidth from eight kilohertz to 512 kilohertz. To improve line settling between bursts, a bandwidth of 20 kilohertz to 512 kilohertz is used. The effective characteristic impedance of 26 AWG telephone twisted pair wire is approximately 110 ohms with an attenuation of 18 decibels-per-kilometer at a frequency of 256 kilohertz. The transformer configuration is shown in Figure 3.

The source impedance resistors for the LO1 and LO2 driver outputs were chosen to be 220 ohms on the transmit tap. This dictates a turns ratio of 2:1 to the line side of the transformer to result in an impedance match to the 110 ohms characteristic impedance of the twisted pair.

To set the 20 kilohertz low-frequency cut off of the transformer interface, the inductance of the transmit winding of the transformer should be 1.75 millihenries. To set the 512

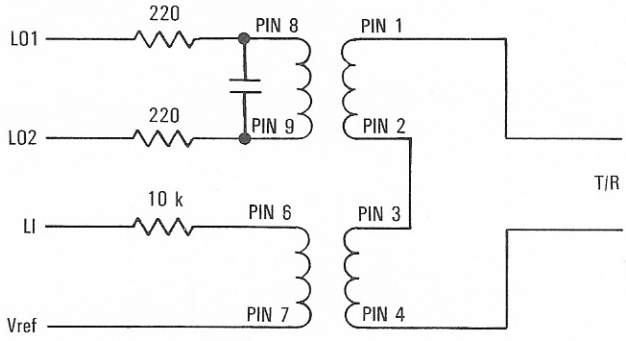


Figure 3. Transformer Configuration

kilohertz high-frequency cut off, a 0.001 microfarads capacitor is connected in parallel with the transmit tap. The turns ratio for the receive winding is determined by the maximum attenuation of the line and the threshold of the receiver detecter. With an initial amplitude of 2.5 volts peak (five volts peak to peak) at LO1 and LO2 halved by the source resistors to 1.25 volts peak at the transmit tap, which is halved again via the turns ratio to the line windings, yields 0.625 volts peak at the line side of the transformer. This 0.625 volts peak is reduced by 36 decibels or a factor of 63 to ten millivolts at the receiving transformer. The receiver of the UDLT has a positive and negative 25 millivolt threshold, which means the receive transformer tap needs a gain of approximately four to meet the needs of the receiver circuitry of the LI pin. This results in the transformer of the schematics, which may be obtained from:

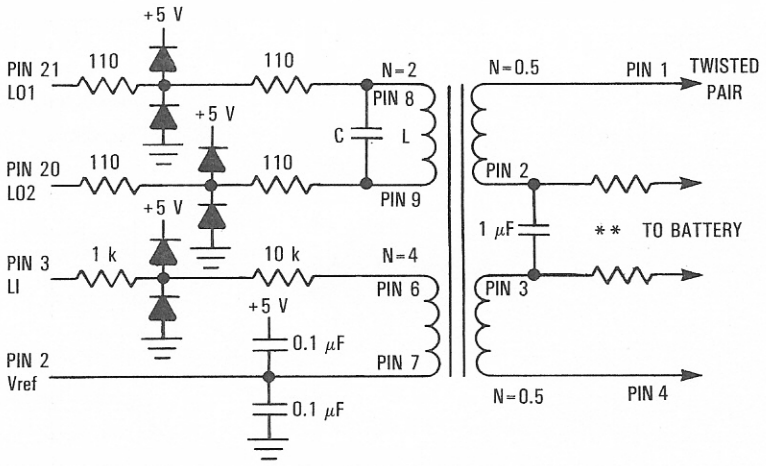
Leonard Electric Products Company
85 Industrial Drive
Brownsville, Texas 78521
P/N P-1358-A

The signals from LO1 and LO2 on the transmit tap are 1.25 volts peak which through the turns ratio to the receive tap becomes 2.5 volts peak at LI. This can exceed the maximum and minimum voltage specification for LI requiring input protection such as the clamping diodes on LI, shown in Figure 4.

When using battery feed through the transformer, further protection is required due to loop current induced spikes at both transmit and receive taps of the transformer. There are several factors to take into consideration when determining the specifications for battery feed current by the center tap of the line side of the transformer. The maximum power is transferred when half of the source voltage is dropped across the effect source resistance. Based on a loop length of two kilometers with a dc resistance of 270 ohms per loop kilometer, a current of 44 milliampheres is the maximum power transfer current. The loop current chosen for the specification is 100 milliampheres. The circuit of Figure 4 is an example of this type of protection.

EVALUATION BOARD DESCRIPTION

The Motorola UDLT evaluation board is a single sided PC board that consists of all the necessary circuitry for end to end operation and demonstration of the 80 kilobits-per-second full duplex synchronous data link of the UDLT master and slave. The evaluation board itself consists of two smaller boards; a master board and a slave board. These two boards may be



** Battery Feed limiting resistors. (optional)

Figure 4. Application Circuit For the Transformer Interface

separated by cutting the panel in half along the two markers, shown in Figure 7. The master board schematic is shown in Figure 5 and the slave board schematic is shown in Figure 6, while the artwork is shown in Figure 7.

The master board contains the master UDLT (MC145422), DSI (MC145428), Mono-circuit (MC14403), the MC1488/1489 or MC145406 RS-232 drivers and receivers, and the necessary clock circuitry to drive these parts. The master board emulates both another digital telset plus the telephone switch interface to the slave board. The master typically is used in the digital switch at the PBX, networked with other digital and analog interface circuits.

The slave board contains the slave UDLT (MC145426), DSI (MC145428), Mono-circuit (MC14402), MC1488/1489, or MC145406 RS-232 Driver/Receiver chips. The slave side emulates a digital telephone where the analog information is digitized at the phone and the information from the phone is digital.

Both master and slave boards have their second eight kilobit signaling channel connected to a DSI for up to 9600 baud of user data simultaneously independent of voice. The baud rates are selected with switches BR1-BR3 (see strapping information). Each board has a DB-25 connector for easy connection to any terminal. Only TxD, RxD, and Ground are connected on the DB-25. Data to and from the DB-25 is fed through the MC1488, MC1489 and the MC145406 Driver/Receiver chips. The socket for the MC145406 RS-232 Driver/Receiver chip is included on each board for evaluation. This part can replace both the driver and receiver chips. Once replaced, the user at his option can cut the MC1488 and MC1489 pads out of the PC board along the dashed lines. This enables each board to fit in a K-2500 phone.

Each board has an RJ-11 socket for easy connection to any modular handset. The signal from each handset is fed through the respective mono-circuit into the 64 kilobit voice channel on the UDLTs. Both master and slave boards have space for a push button switch which can be hardwired onto the SI1, along with an LED on SO1 for signaling on channel one. This channel is optional to the user and can be used with a microprocessor in the phone or a pulse dialer. Signaling bits one and two provide eight kilobits-per-second each of protocol independent data. Switches permit access to particular features of the voice/data integrated circuits on both boards, as explained below.

STRAPPING INFORMATION

The component layout is shown in Figure 8. The layout shows the footprints for switches which can be used with wire straps. The solid lines indicate the normal strap positions which; select Mu law, 9600 baud data rate, with one start bit, eight data bits and one stop bit. The dip switches can be used if desired and can be obtained from:

Grayhill Inc.
561 Hillgrove Avenue
La Grange, Illinois 60525

P/N	Name	Qty
78J05	S1, S2	3
78J02	S3	1

STRAPPING ON THE MASTER

S1 — These straps select via U2 (MC145428 DSI) the number of stop bits, the length of the data word and the baud rate selected for the asynchronous data.

SW1 — (SB) A high selects two stop bits; a low selects one stop bit.

SW2-SW4-(BR3-BR1) — These bit rate inputs select the asynchronous bit rate, either externally supplied at the BC pin (16 times clock) or one of the supplied bit rates shown in the table on page 2-309 of the Telecommunications data book.

SW5 — (DL) This Data Length input pin selects a nine bit data word when high or an eight bit word when low.

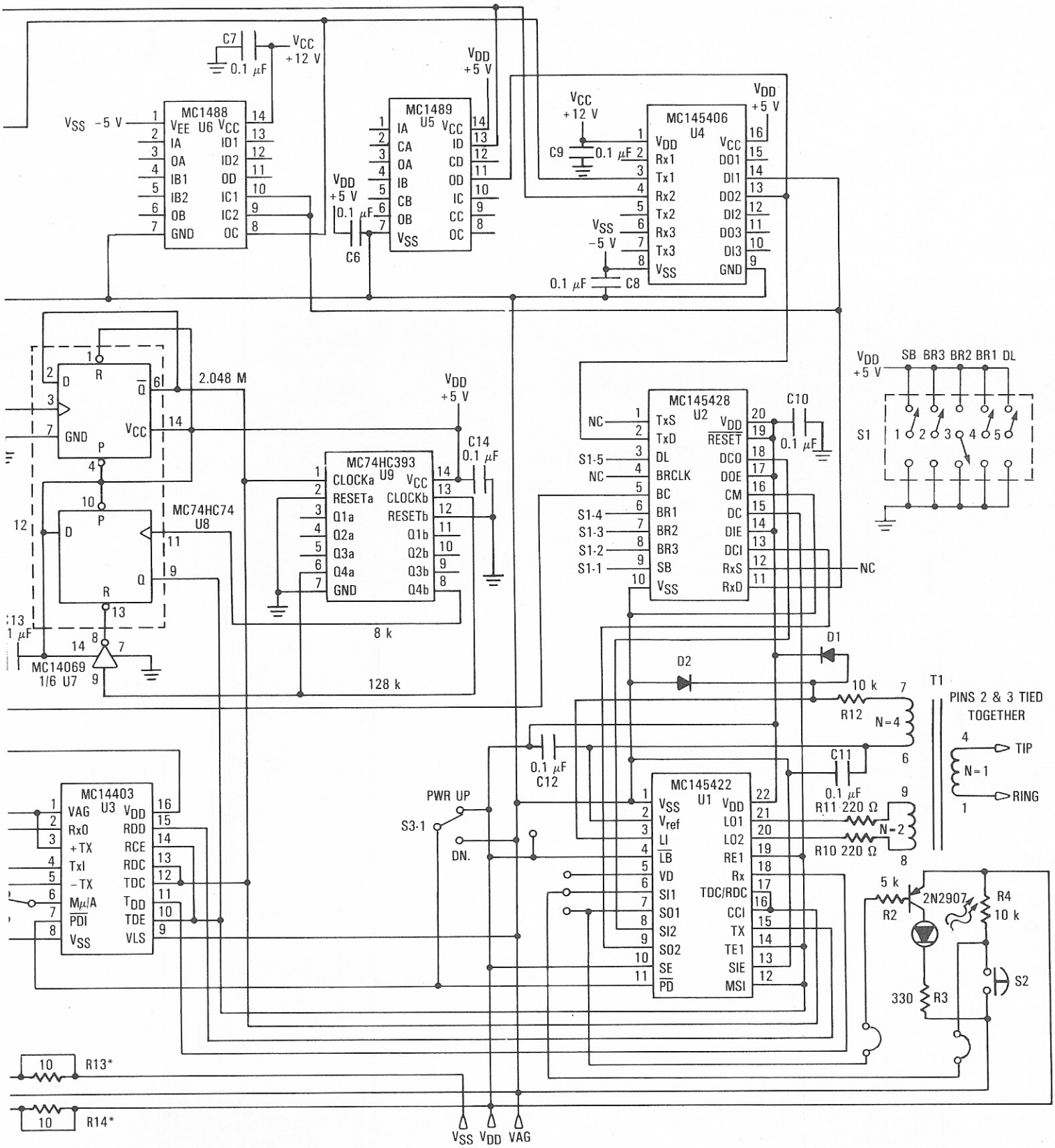


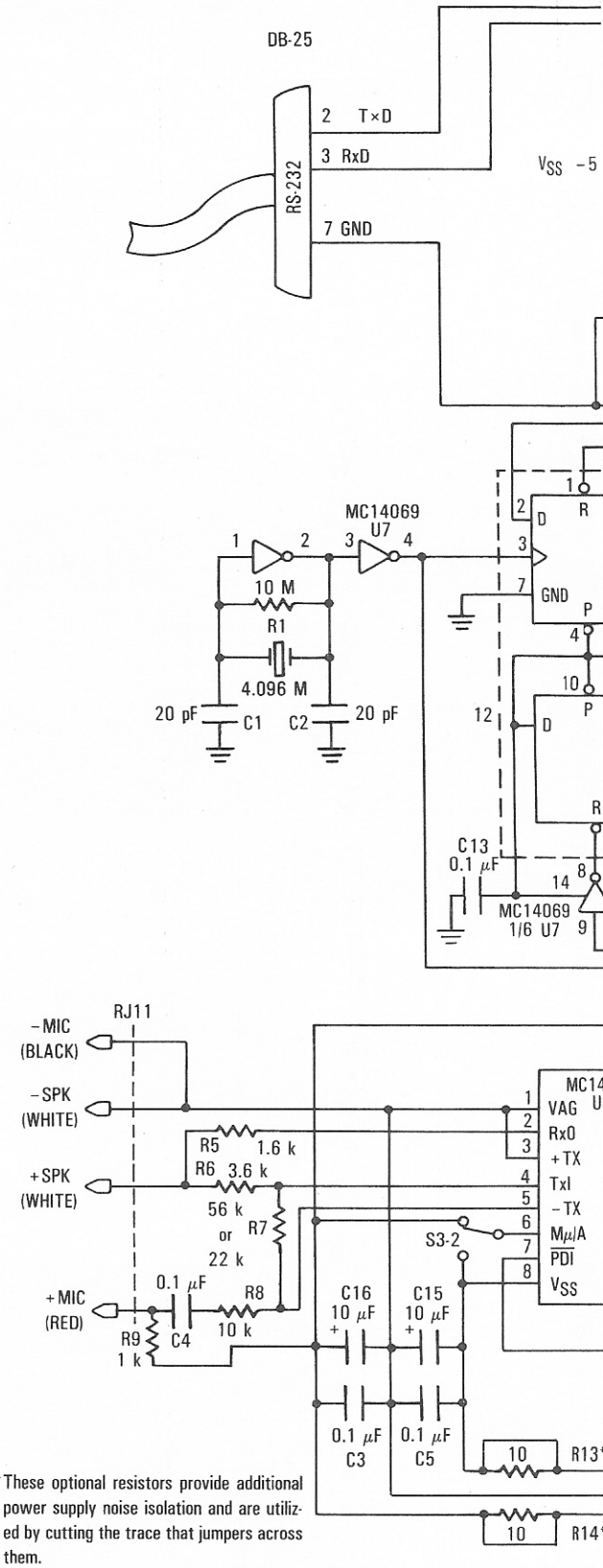
Figure 5. Master UDLT Demo Board

MASTER UDLT DEMO BOARD PARTS LIST

PART	QUANTITY (PART NUMBER)
MC145422	1-U1
MC145428	1-U2
MC14403	1-U3
MC145406	1-U4
MC1489	1-U5
MC1488	1-U6
MC14069UB	1-U7
MC74HC74	1-U8
MC74HC393	1-U9
LEPCO P-1358A	1-T1
DB25	1
RJ11	1
GRAYHILL (SPDT 78J05)	1-S1
CUTLER-HAMMER B8500W/PZ81R	1-S2
GRAYHILL (SPDT 78J02)	1-S3
BANANA JACKS	6
20 pF	2-C1 & C2
0.1 μF	12-C3-C14
10 μF	2-C15, C16
10 M	1-R1
5 K	1-R2
330 Ω	1-R3
1.6 K	1-R5
3.6 K	1-R6
56 K	1-R7
10 K	1-R8
1 K	1-R9
220 Ω	2-R10, R11
10 K	2-R12, R4
10 Ω	2-R13, R14
CRYSTAL	1-4.096 M
JUMPERS	10
DIODES 1N914	2-D1, D2
LED (T1)	1
2N2907	1

SOLDER TAIL SOCKETS

14 PIN	5
16 PIN	2
20 PIN	1
22 PIN	1



*These optional resistors provide additional power supply noise isolation and are utilized by cutting the trace that jumpers across them.

S2 — This switch is optional and is hardwired to signaling channel one for demonstration using LEDs. The footprint for this switch is included on the board.

This switch can be obtained from:

Cutler-Hammer
P/N B8500W/P281R

S3 — These straps select Mu or A laws and power down on the MC14403 Mono-circuit and MC145422 master UDLT.

SW1 — (PD) This strap when high, powers both the mono-circuit and master UDLT. When low, both parts are powered down.

SW2 — (Mu/A) Selects Mu or A law coding.

Loopback and Valid Data on the master can be accessed via pads.

STRAPPING ON THE SLAVE

S1 — Same as S1 on the master; selects asynchronous data format and bit rate.

S2 — These straps select Tone Enable, Power Down, Mu/A, and Loopback features of the slave (MC145426) as well as Mu/A and Power Down on the MC14402 Mono-circuit.

SW1 — (TE) A high enables a 500 hertz tone.

SW2 — ($\overline{PD}$) Powers both the slave and mono-circuit up or down. High = powered up, and Low = powered down.

SW3 — (Mu/A) Selects Mu or A law coding for the mono-circuit.

SW4 — (Mu/A) Selects Mu or A law coding for the slave UDLT.

SW5 — (LB) When low, the 64 kilobits-per-second of information coming from the master will loop through the slave and return to the master. The signaling bits are unaffected.

S3 — Same as the S2 switch on the master.

POWER SUPPLY CONSIDERATIONS/LAYOUT GUIDELINES

The power supply requirements for these boards are V_{DD} at +5 volts, V_{SS} at −5 volts and V_{CC} which is the RS-232 driver positive voltage of +7 to +12 volts for the MC1488. V_{CC} may be as low as +5 volts with the MC145406 Driver/Receiver chip. The power supply current required by each of these voltages is less than 30 milliamperes. This results in a total slave board power consumption of less than 400 milliwatts. This amount of power may be supplied by the loop using a linear supply. To isolate the RS-232 port with respect to earth ground, a switching regulator powered by the loop or an external power supply will be required. If a switching regulator is used, it should be synchronized to the eight kilohertz and 128 kilohertz clocks of the slave UDLT to reduce the affects of aliasing noise into the analog circuitry of either the UDLT or audio voice channel. This function will be supported by the MC34129 Digital Telephone Switching Power Supply Controller chip. This device has the capability to power-up and regulate on its internal oscillator. After regulation is established it can synchronize to an external clock such as the slave's 128 kilohertz clock.

SLAVE UDLT DEMO BOARD PARTS LIST

PART	QUANTITY (PART NUMBER)	PART	QUANTITY (PART NUMBER)
MC145426	1-U1	500 Ω	1-R6
MC145428	1-U2	10 K	1-R7
MC14402	1-U3	56 K	1-R8
MC145406	1-U4	220 Ω	2-R9, R10
MC1489	1-U5	10 K	3-R11, R13, R2
MC1488	1-U6	1 K	1-R12
LEPCO P-1358A	1-T1	10 Ω	2-R14, R15
DB25	1	JUMPERS	12
RJ11	1	CRYSTAL	1-4.096 M
GRAYHILL (SPDT 78J05)	2-S1 & S2	LED (T1)	1
CUTLER-HAMMER B8500W/P281R	1-S3	DIODES 1N914	2-D1, D2
BANANA JACKS	6	2N2907	1
20 pF CAPS	2-C1 & C2		
0.1 μF CAPS	10-C3-C11, C14	**SOLDER TAIL SOCKETS**	
10 μF CAPS	2-C12, C13	14 PIN	2
10 M	1-R1	16 PIN	1
5 K	1-R3	20 PIN	1
330 Ω	1-R4	22 PIN	2
5 K	1-R5		

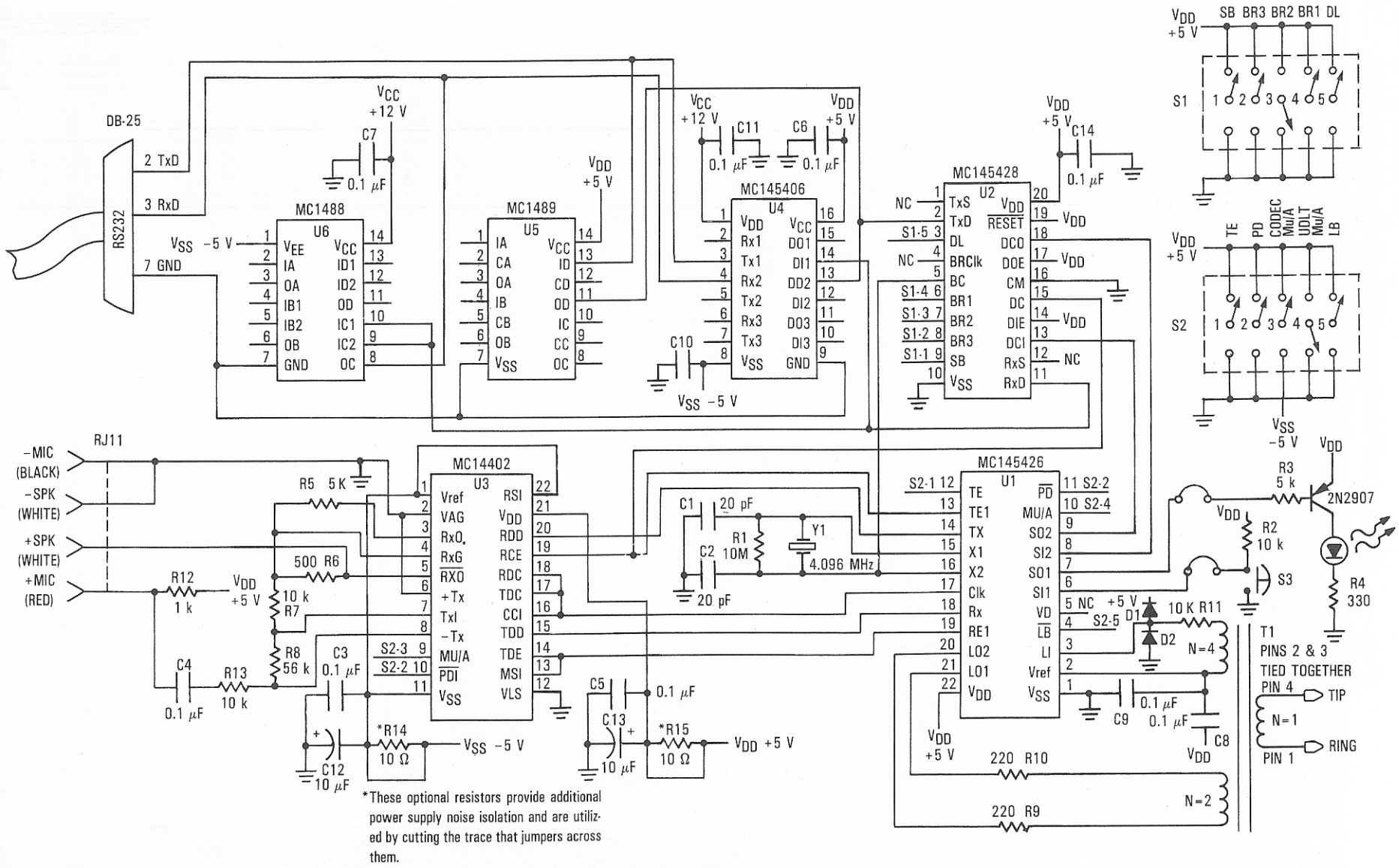


Figure 6. Slave UDLT Demo Board

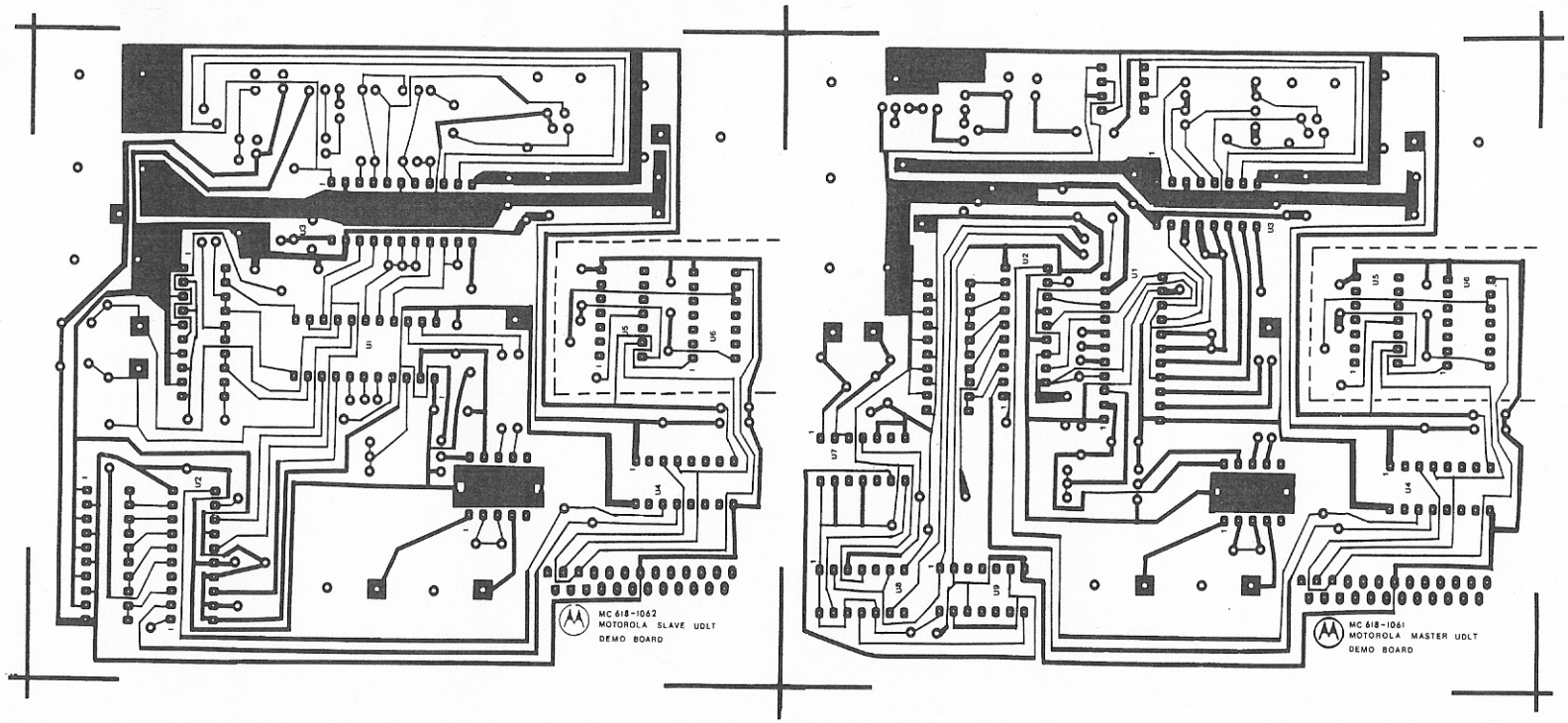


Figure 7. Artwork of UDLT Voice/Data Evaluation Board

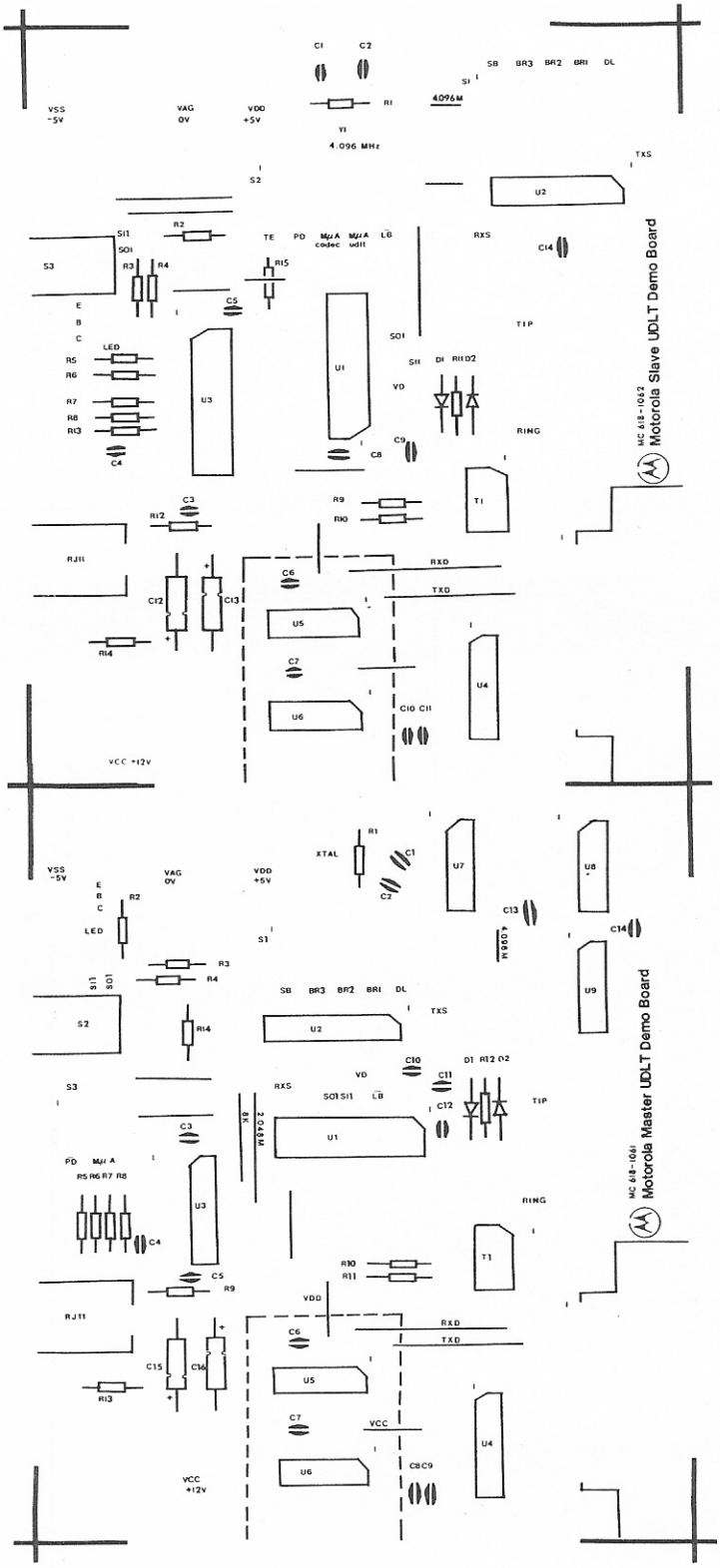


Figure 8. Component Layout

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

EUROPE: Motorola Ltd.; European Literature Center; Fairfax House; 69 Buckingham Ct.; Aylesbury Bucks; HP202NF United Kingdom.

HONG KONG: Motorola Inc.; International Semiconductor Group; P.O. Box 80300; Cheung Sha Wan Post Office; Hong Kong.

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