AN1277

Offset Reference PLLs for Fine Resolution or Fast Hopping

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INTRODUCTION

Frequency synthesis by use of two loops, with reference frequencies offset from each other, can provide much finer resolution or faster hopping than a single loop. Dual PLL ICs are available to make compact low–current synthesizers using the technique.

Alternative techniques will be discussed, the design method described, and examples provided. This technique has been used successfully with the Motorola MC145220 dual PLL, providing 10 Hz step size, 30 MHz frequency range, and switching time of 30 ms.

ALTERNATIVE TECHNIQUES

DIRECT DIGITAL SYNTHESIS

Direct Digital Synthesis (DDS) composes a sine wave from discrete digitized samples. Sometimes they are called Numerically Controlled Oscillators (NCOs). Samples for one complete sine wave are stored in read only memory (ROM). A clock outputs a sample every period. At some frequency every sine wave sample will be used. At a higher frequency every second or third sample might be used. Digital to analog conversion produces analog levels corresponding to sample codes. The output is low pass filtered. Below 1 Hz resolution and micro–second switching are the advantages of DDS.

Spurious signal levels and high current are the weaknesses. Currently available digital to analog converters have spurious levels greater than – 76 dB in the VHF and higher frequency range. Sometimes manufacturers of DDS devices that do not include a D/A converter will give specs that are computed assuming the D/A is perfect. Spurious of – 96 dB could be quoted under these conditions. Spurious signal levels make DDS unsuitable for most receiver and many transmitter applications. Current consumption is greater than 100 mA.

FRACTIONAL N

It is possible to have PLL output increments smaller than the step size by use of a fractional N divider in the feedback loop. Available fractional N ICs cannot achieve 1000 times ratio of loop step size to output increment. The offset reference technique can do it. Fractional N synthesis produces spurious signals at the increment offset from the carrier. Offset reference does not do this.

TRIPLE LOOP PLLs

Triple loop PLLs are the most common technique used to obtain an output that increments in steps much smaller than the step size of the individual loops. An example is shown in Figure 1. The output tunes 45 – 75 MHz in 10 Hz steps to convert the 0 – 30 MHz HF spectrum onto a 45 MHz IF.

An offset loop operates 44 – 74 MHz in 100 kHz steps. The fine tune loop covers 1.0 – 1.1 MHz. A 45 – 75 MHz VCO is phase locked to the sum frequency of the offset and fine tune PLLs. Fine tune loop frequency range is always equal to the step size of the offset loop.

Phase lock in the output loop depends on phase lock in the two other loops, the mixer output being initially within the filter passband, and output loop VCO being at a higher frequency than the offset loop. Two situations can cause the output loop to latch up with the other two loops locked. If the VCO is too high in frequency initially, filter output is not enough to drive the phase detector. Phase detector output (PD_{out}) goes high and pulls the VCO further from lock. If the VCO initially is below the offset loop, the PD_{out} line tunes it away from lock.

Lock detect (LD) from the output loop detects latch–up. If the loop hasn't locked within a set amount of time, the VCO sweep circuit moves the VCO through its operating range. During frequency changes, all four transient phenomena can occur. The triple loop PLL is not simple to design and produce.

OFFSET REFERENCE PLL ADVANTAGES

The offset reference PLL (Figures 2 and 3) use two loops mixed together to produce an output with a smaller step size than the individual loops. The reference frequency difference between the two phase detectors is the output step size. Compared to the triple loop, it avoids loop latch–up, uses one less PLL, and can be designed with each PLL operating independently.

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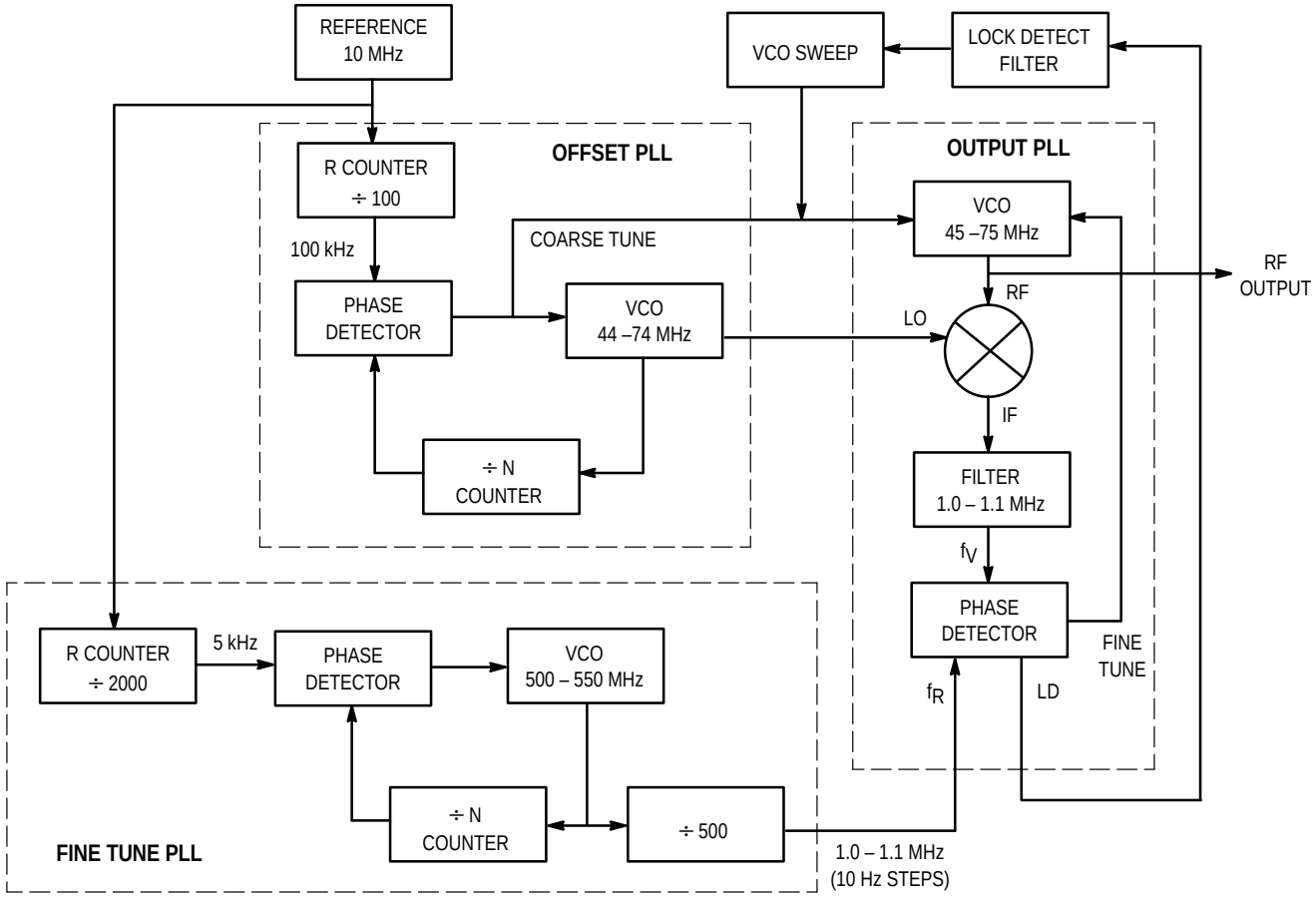

Figure 1. 45 – 75 MHz Triple PLL Synthesizer

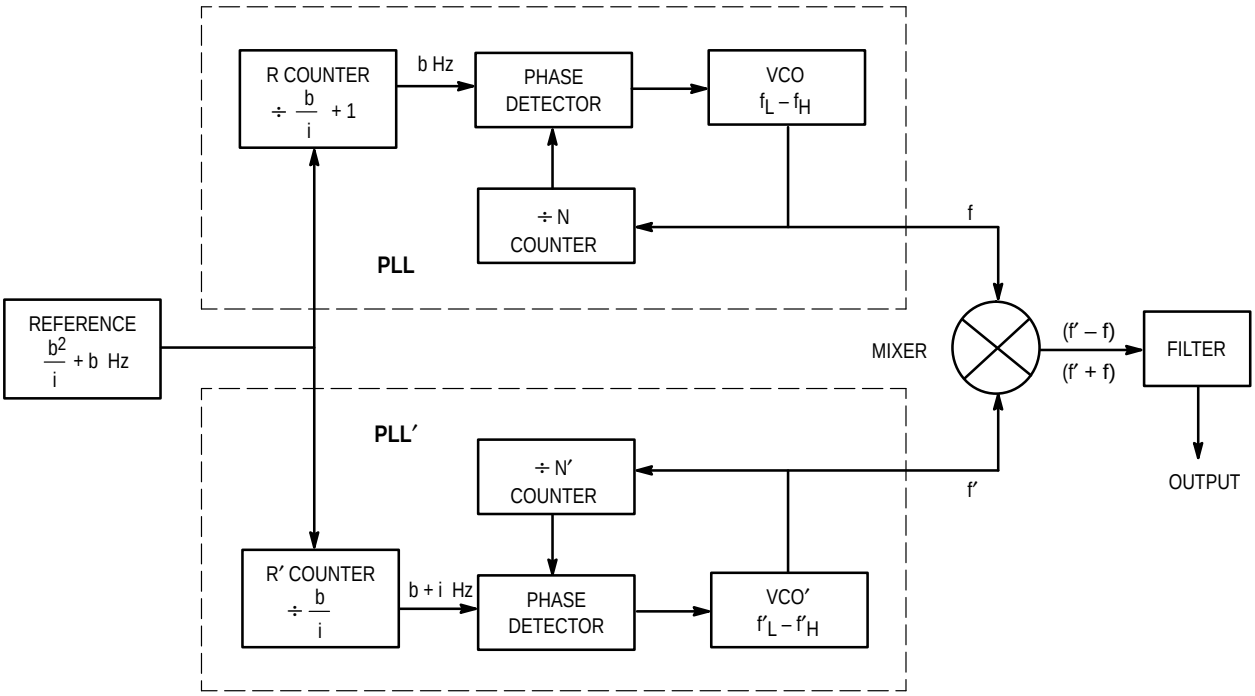

Figure 2. Output Mixed PLLs

COMMON CHARACTERISTICS

Table 1. Variable Definitions

Variable	Definition
b	Step Size of PLL–Base Step Size
i	Step Size of Synthesized Output (f′ – f), (f′ +f), or f, Depending on Configuration
b + i	Step Size of PLL′
C	Reference Frequency
(f′ – f)	Mixer Difference Frequency Output
(f′ + f)	Mixer Sum Frequency Output
$(f' - f)_L$	Low Frequency Limit of (f′ – f)
$(f' - f)_H$	High Frequency Limit of (f′ – f)
$(f' + f)_L$	Low Frequency Limit of (f′ + f)
$(f' + f)_H$	High Frequency Limit of (f′ + f)
R, R′	Reference Divider Values
N, N′	PLL, PLL′ Feedback Divider Values
N'_L, N'_H	Lowest and Highest N′ Divider Values
N'_{imax}	Number of N′ Divider Values Used in Addition to N'_L
f, f′	VCO, VCO′ Frequency
f_L, f'_L	VCO, VCO′ Lowest Frequency
f_H, f'_H	VCO, VCO′ Highest Frequency

N, N′ COUNT SEQUENCE EXCEPT FEEDBACK SUM CONFIGURATION

At any output frequency that is an integer multiple of the base step size (b), $f' = f'_L$. As the output is stepped up in frequency by increment (i), the N′ counter is incremented by one in the sequence $N'_L...N'_H$. N'_H is the counter value one increment (i) below the next output frequency, which is an integer multiple of (b).

Through the $N'_L...N'_H$ count sequence, N either increments or decrements by one each time the output frequency is stepped up by (i). The term in the output frequency equation which is multiplied by (b) will be held constant. At the same time, the term multiplied by (i) will be increased.

N, N′ COUNT SEQUENCE FEEDBACK SUM CONFIGURATION

At any output frequency that is an integer multiple of the base step size (b), $f' = f'_H$. As the output is stepped up in frequency by increment (i), the N′ counter decrements by one in the sequence $N'_H...N'_L$. N'_L is the counter value one increment (i) below the next output frequency, which is an integer multiple of (b).

Through the $N'_H...N'_L$ count sequence, N decrements by one each time the output frequency is stepped up by (i). The term in the output frequency equation which is multiplied by (b) will be held constant. At the same time, the term multiplied by (i) will be increased.

FORMULA LIMITATIONS

There are a few restrictions on PLL and PLL′ frequencies which were made only to simplify the formulas.

Both the output and feedback mixed difference frequency configurations require $f'_L > f_H$ so that as the output increases in frequency, the N′ counter value increments.

Output frequency endpoints and either f'_L or f'_H are integer multiples of the base step size (b). This ensures that at the endpoints, VCO′ is at f'_L or f'_H. VCO′ is also at f'_L or f'_H for any output frequency between the endpoints that can be evenly divided by (b). If the conditions were not met, N′ could be anywhere in its count cycle at endpoints. Adding terms to the equations for the two VCO tuning ranges would allow endpoints to be multiples only of the incremental step size (i).

Reference frequency C is given for the lowest frequency that can produce both step sizes by integer division. The R divide value will be one greater than the R′ divider. Any reference frequency can be used that is a multiple of the C value from the table.

Since either f'_L or f'_H and C divide by both step sizes, f'_L or f'_H will be an integer multiple of C.

Table 2. Formulas For All Configurations

Variable	Design Equations
C	$C = \frac{b^2}{i} + b$ or $C = \frac{b}{i}(b + i)$
R	$R = \frac{b}{i} + 1$
R′	$R' = \frac{b}{i}$
N'_{imax}	$N'_{imax} = \frac{b}{i} - 1$
N'_H	$N'_H = N'_L + N'_{imax}$
f′	$f' = N'(b + i)$
$f'_H - f'_L$	$f'_H - f'_L = \frac{b^2}{i} - i$
f'_H	$f'_H = f'_L + \frac{b^2}{i} - i$

OUTPUT MIXED PLLs

Table 3. Output Mixed (f′ – f) Formulas

Variable	Design Equations
$(f' - f)$	$(f' - f) = b(N' - N) + N'i$
$(f' - f)_L$	$(f' - f)_L = f'_L - f_H + N'_{imax}b$
$(f' - f)_H$	$(f' - f)_H = f'_L - f_L$
f'_L	Any frequency for which $f'_L > f_H$ and f'_L is an integer multiple of C
f	$f = Nb$
f_L	$f_L = f'_L - (f' - f)_H$
f_H	$f_H = f'_L - (f' - f)_L + N'_{imax}b$
$f_H - f_L$	$f_H - f_L = (f' - f)_H - (f' - f)_L + N'_{imax}b$

OUTPUT (f′ – f) KEY POINTS

(a) RF output is (f′ – f) with $f'_L > f_H$.
(b) C and f'_L divide evenly by both step sizes.
(c) f_L, f_H, $(f' - f)_L$, $(f' - f)_H$ divide evenly by b.

OUTPUT (f′ – f) EXAMPLE

The desired frequency range is 150 – 154 MHz in 0.5 MHz steps using PLLs with 2.0 MHz and 2.5 MHz step sizes.

Reference frequency:

$$C = \frac{b^2}{i} + b = \frac{2^2}{0.5} + 2 = 10 \text{ MHz}$$

The reference divider values are:

$$R = \frac{b}{i} + 1 = \frac{2}{0.5} + 1 = 5$$

$$R' = \frac{b}{i} = \frac{2}{0.5} = 4$$

The number of N′ counter values used in addition to N'_L is:

$$N'_{imax} = \frac{b}{i} - 1 = \frac{2}{0.5} - 1 = 3$$

The frequency range of VCO′ is:

$$f'_H - f'_L = \frac{b^2}{i} - i = \frac{2^2}{0.5} - 0.5 = 7.5 \text{ MHz}$$

The frequency range of VCO is:

$$f_H - f_L = (f' - f)_H - (f' - f)_L + N'_{imax}b$$
$$= 154 - 150 + 3(2)$$
$$= 10 \text{ MHz}$$

f'_L and f_H frequencies depend on each other. To select values, the equation for f_H is solved in terms of f'_L:

$$f_H = f'_L - (f' - f)_L + N'_{imax}b$$
$$= f'_L - 150 + 3(2)$$
$$= f'_L - 144$$

Frequencies used for f'_L and f_H are a tradeoff between phase noise and ease of filtering the mixer products. As f'_L and f_H increase, filtering of mixer products improves. However, the VCO noise increases. The same VCO resonator Q at a higher frequency results in higher noise for the same offset frequency. PLL ICs also produce more noise with increasing frequency.

f'_L of 500 MHz is chosen. The frequency range of VCO′ is 500 – 507.5 MHz. The frequency range of VCO is 346 – 356 MHz.

To check results, all divide values and frequencies are in Table 4.

Table 4. Output Mixed (f′ – f) Example

(f′ – f) MHz	N	N′	f MHz	f′ MHz
150	175	200	350	500
150.5	176	201	352	502.5
151	177	202	354	505
151.5	178	203	356	507.5
152	174	200	348	500
152.5	175	201	350	502.5
153	176	202	352	505
153.5	177	203	354	507.5
154	173	200	346	500

Table 5. Output Mixed (f′ + f) Formulas

Variable	Design Equations
(f′ + f)	(f′ + f) = b(N′ + N) + N′i
$(f' + f)_L$	$(f' + f)_L = f_L + f'_L + N'_{imax}b$
$(f' + f)_H$	$(f' + f)_H = f_H + f'_L$
f'_L	Any frequency f'_L which is an integer multiple of C
f	f = Nb
f_L	$f_L = (f' + f)_L - f'_L - N'_{imax}b$
f_H	$f_H = (f' + f)_H - f'_L$
$f_H - f_L$	$f_H - f_L = (f' + f)_H - (f' + f)_L + N'_{imax}b$

OUTPUT (f′ + f) KEY POINTS

(a) RF output is (f′ + f).
(b) C and f'_L divide evenly by both step sizes.
(c) f_L, f_H, $(f' + f)_L$, $(f' + f)_H$ divide evenly by b.

OUTPUT (f′ + f) EXAMPLE

The desired frequency range is 800 – 801 MHz in 125 kHz steps using PLLs with 500 kHz and 625 kHz step sizes.

Reference frequency:

$$C = \frac{b^2}{i} + b = \frac{500^2}{125} + 500 = 2.5 \text{ MHz}$$

The reference divider values are:

$$R = \frac{b}{i} + 1 = \frac{500}{125} + 1 = 5$$

$$R' = \frac{b}{i} = \frac{500}{125} = 4$$

The number of N′ counter values used in addition to N'_L is:

$$N'_{imax} = \frac{b}{i} - 1 = \frac{500}{125} - 1 = 3$$

The frequency range of VCO′ is:

$$f'_H - f'_L = \frac{b^2}{i} - i = \frac{500^2}{125} - 125 = 1.875 \text{ MHz}$$

The frequency range of VCO is:

$$f_H - f_L = (f' + f)_H - (f' + f)_L + N'_{imax}b$$
$$= 801 - 800 + 3(0.5)$$
$$= 2.5 \text{ MHz}$$

f'_L and f_H frequencies depend on each other. To select values, the equation for f_H is solved in terms of f'_L:

$$f_H = (f' + f)_H - f'_L \text{ or } f_H = 801 - f'_L$$

Frequencies used for f'_L and f_H are a tradeoff between phase noise and ease of filtering the undesired mixer products. The best filtering of spurious mixer products occurs if both VCOs are operating at about half the desired output frequency. This increases the frequency separation of the sum and difference products. VCO noise increases with frequency. The same VCO resonator Q at a higher frequency results in higher noise for the same offset frequency. PLL ICs also produce more noise with increasing frequency.

f'_L of 400 MHz is chosen. The frequency range of VCO′ is 400 – 401.875 MHz. The frequency range of VCO is 398.5 – 401 MHz.

To check results, all divide values and frequencies are in Table 6.

Table 6. Output Mixed (f′ + f) Example

(f′ + f) MHz	N	N′	f MHz	f′ MHz
800	800	640	400	400
800.125	799	641	399.5	400.625
800.25	798	642	399	401.25
800.375	797	643	398.5	401.875
800.5	801	640	400.5	400
800.625	800	641	400	400.625
800.75	799	642	399.5	401.25
800.875	798	643	399	401.875
801	802	640	401	400

FEEDBACK MIXED PLLs

Table 7. Feedback (f′ – f) Formulas

Variable	Design Equations
f	$f = b(N' - N) + N'i$
f'_L	Any frequency for which $f'_L > f_H$ and f'_L is an integer multiple of C
$(f' - f)_L$	$(f' - f)_L = f'_L - f_H$
$(f' - f)_H$	$(f' - f)_H = f'_L - f_L + N'_{imax}b$
$(f' - f)_H - (f' - f)_L$	$(f' - f)_H - (f' - f)_L = f_H - f_L + N'_{imax}b$

FEEDBACK (f′ – f) KEY POINTS

(a) RF output is f with $f'_L > f_H$.
(b) C and f'_L divide evenly by both step sizes.
(c) f_L, f_H, $(f' - f)_L$, $(f' - f)_H$ divide evenly by b.
(d) Feedback mixer output is (f′ – f).

FEEDBACK (f′ – f) EXAMPLE

The desired frequency range is 63 – 64 MHz in 100 kHz steps using PLLs with 500 kHz and 600 kHz step sizes.

Reference frequency:

$$C = \frac{b^2}{i} + b = \frac{500^2}{100} + 500 = 3 \text{ MHz}$$

The reference divider values are:

$$R = \frac{b}{i} + 1 = \frac{500}{100} + 1 = 6$$

$$R' = \frac{b}{i} = \frac{500}{100} = 5$$

The number of N′ counter values used in addition to N'_L is:

$$N'_{imax} = \frac{b}{i} - 1 = \frac{500}{100} - 1 = 4$$

The frequency range of VCO′ is:

$$f'_H - f'_L = \frac{b^2}{i} - 1 = \frac{500^2}{100} - 100 = 2.4 \text{ MHz}$$

The frequency range of VCO is the output frequency range, which is 63 – 64 MHz.

f'_L is selected such that $f'_L > f_H$ and f'_L is an integer multiple of C. If the frequency ranges for VCO and VCO′ are close together, sum and difference products from the mixer will be further apart and easier to filter.

If both VCOs operate at close to the output frequency, they might overlap. Mixer output could be (f – f′) and VCO would be pulled in the wrong direction.

f'_L of 66 MHz is chosen. The frequency range of VCO′ is 66 – 68.4 MHz. N counter input frequency range is:

$$(f' - f)_L = f'_L - f_H$$
$$= 66 - 64$$
$$= 2 \text{ MHz}$$

$$(f' - f)_H = f'_L - f_L + N'_{imax}b$$
$$= 66 - 63 + 4(0.5)$$
$$= 5 \text{ MHz}$$

To check results, all divide values and frequencies are in Table 8.

Table 8. Feedback (f′ – f) Example

(f′ – f) MHz	N	N′	f MHz	f′ MHz
3	6	110	63	66
3.5	7	111	63.1	66.6
4	8	112	63.2	67.2
4.5	9	113	63.3	67.8
5	10	114	63.4	68.4
2.5	5	110	63.5	66
3	6	111	63.6	66.6
3.5	7	112	63.7	67.2
4	8	113	63.8	67.8
4.5	9	114	63.9	68.4
2	4	110	64	66

Table 9. Feedback (f′ + f) Formulas

Variable	Design Equations
f	$f = b(N - N') - N'i$
f'_H	f'_H is an integer multiple of C
$(f' + f)_L$	$(f' + f)_L = f'_L + f_L + N'_{imax}i$
$(f' + f)_H$	$(f' + f)_H = f_H + f'_H$
(f′ + f)	(f′ + f) = Nb

FEEDBACK (f′ + f) KEY POINTS

(a) RF output is f.
(b) C and f'_H divide evenly by both step sizes.
(c) f_L, f_H, $(f' + f)_L$, $(f' + f)_H$ divide evenly by b.

FEEDBACK (f′ + f) EXAMPLE

The desired frequency range is 63 – 64 MHz in 100 kHz steps using PLLs with 500 kHz and 600 kHz step sizes.

Reference frequency:

$$C = \frac{b^2}{i} + b = \frac{500^2}{100} + 500 = 3 \text{ MHz}$$

The reference divider values are:

$$R = \frac{b}{i} + 1 = \frac{500}{100} + 1 = 6$$

$$R' = \frac{b}{i} = \frac{500}{100} = 5$$

The number of N′ counter values used in addition to N'_H is:

$$N'_{imax} = \frac{b}{i} - 1 = \frac{500}{100} - 1 = 4$$

The frequency range of VCO′ is:

$$f'_H - f'_L = \frac{b^2}{i} - i = \frac{500^2}{100} - 100 = 2.4 \text{ MHz}$$

The frequency range of VCO is the output frequency range, which is 63 – 64 MHz.

f'_H is selected to be an integer multiple of C. If the frequency ranges for VCO and VCO′ are close together, sum and difference products from the mixer will be further apart and easier to filter.

f'_H of 66 MHz is chosen. The frequency range of VCO′ is 63.6 – 66 MHz.

The frequency limits of the input to the N counter are:

$$(f' + f)_L = f'_L + f_L + N'_{imax}i$$
$$= 63.6 + 63 + 4(0.1)$$
$$= 127 \text{ MHz}$$

$$(f' + f)_H = f_H + f'_H$$
$$= 64 + 66$$
$$= 130 \text{ MHz}$$

To check results, all divide values and frequencies are in Table 10.

Table 10. Feedback (f′ + f) Example

(f′ + f) MHz	N	N′	f MHz	f′ MHz
129	258	110	63	66
128.5	257	109	63.1	65.4
128	256	108	63.2	64.8
127.5	255	107	63.3	64.2
127	254	106	63.4	63.6
129.5	259	110	63.5	66
129	258	109	63.6	65.4
128.5	257	108	63.7	64.8
128	256	107	63.8	64.2
127.5	255	106	63.9	63.6
130	260	110	64	66

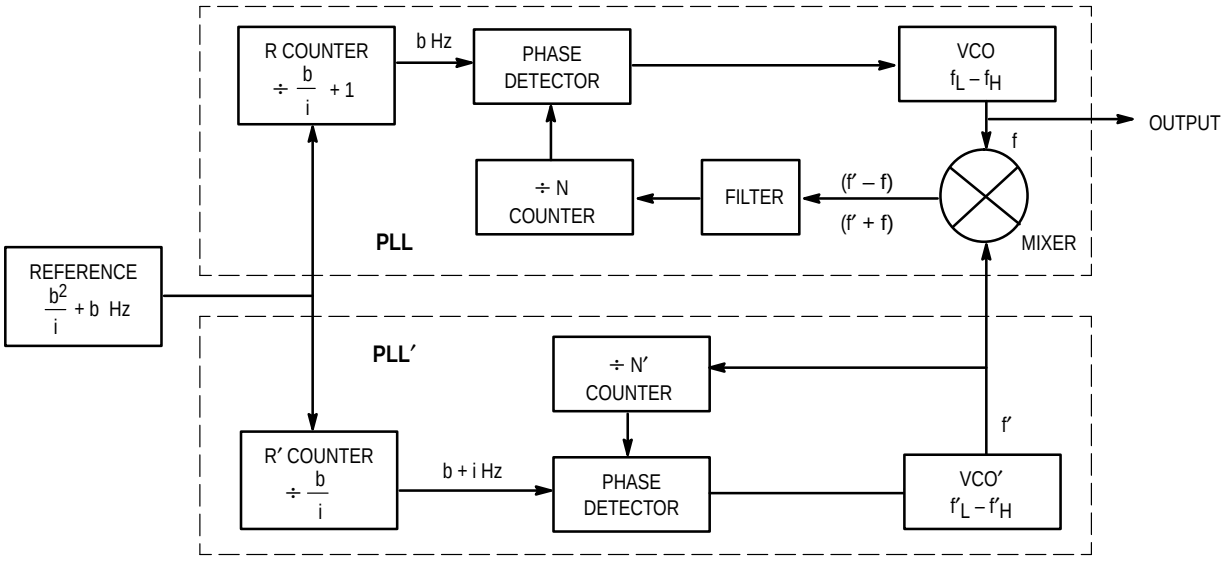

Figure 3. Feedback Mixed PLLs — f Output

DESIGN TRADEOFFS

LIMITATIONS OF FEEDBACK SUM

Feedback sum output causes the N counter to operate at a higher frequency than the desired output. Phase noise within the loop bandwidth could be up to 8 – 9 dB worse than the feedback difference circuit. The worst case for phase noise is the best case for spurious product suppression from the mixer. (Both VCOs operate at about the same frequency.)

OUTPUT MIXED DIFFERENCE

At least one VCO will operate at frequencies above the desired output. This is most useful where the output tuning range is a high percentage of the center frequency. Frequencies of DC – 100 MHz, for example, would be simple to implement in this configuration. If the feature is not needed, phase noise will be higher than necessary.

FEEDBACK DIFFERENCE

This technique results in low phase noise and avoids mixer products being in the output. It works well when both VCOs can tune the ranges needed without range switching. Output mixed sum should also be considered.

OUTPUT MIXED SUM

If the output is between 400 MHz and 800 MHz, it may be better to use two JFET VCOs and sum the outputs. Two bipolar VCOs combined using feedback difference might have higher phase noise. The loops also function independently.

OUTPUT VS. FEEDBACK MIXING

Output mixing allows both PLLs to operate independently. Spurious mixer products will be present on the output. Feedback mixing results in the products being on the PLL input where they will need much less filtering. Also the switching time and damping may depend on both PLLs.

The total number of N′ counter values used is:

$$N'_{Total} = \frac{b}{i}$$

Due to N'_{Total}, it is quite likely that the tuning range of VCO′ is much smaller than that of VCO. VCO′ would then frequency hop much more quickly. The frequency switching characteristics of PLL using feedback mixing might not be dependent on PLL′.

FREQUENCY RANGE EXTENSION

Both the output mixed sum and feedback mixed difference PLLs can extend the frequency range of the PLL ICs they are used with by approximately two times. Both VCOs would need to be on about the same frequency.

SUMMARY

A series of examples and equations has been described to illustrate a technique that, though not commonly applied, is an elegant way to achieve fine resolution and faster switching.

Offset reference PLLs have become much easier to implement since the introduction of dual loop PLL ICs such as the Motorola MC145220, which operates from 40 MHz – 1.1 GHz. Phase detector and reference divider maximum input frequencies are the major limitation on (b) to (i) ratio.

The MC145220 EVK (Evaluation Kit) implements the output mixed difference technique to achieve 30 ms switching from 60 – 80 MHz. After the switching time has elapsed, the output is within 1 kHz of final frequency. PLL has 10 kHz steps and PLL′ has 10.01 kHz steps. Output increment size is 10 Hz. 10 kHz sideband levels are – 80 dB.

ACKNOWLEDGEMENT

1. Jim Irwin of Motorola Semiconductor Products Sector provided many examples of alternative multiple loop schemes.

REFERENCE

2. *Communications Device Data* (DL136/D Rev. 4), page 2–605, Motorola, 1995. Figure 11 is a sample PLL by John Hatchett using the offset reference technique.

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